ViRGE/MX Dual Display Accelerator

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NOTATIONAL CONVENTIONS

The following notational conventions are used in this data book:

Signal names are shown in all uppercase letters. For example, XD.

A bar over a signal name indicates an active low signal. For example, $\overline{OE}$.

n-m indicates a bit field from bit n to bit m. For example, 7-0 specifies bits 7 through 0, inclusive.

n:m indicates a signal (pin) range from n to m. For example D[7:0] specifies data lines 7 through 0, inclusive

Use of a trailing letter H indicates a hexadecimal number. For example, 7AH is a hexadecimal number.

Use of a trailing letter b indicates a binary number. For example, 010b is a binary number.

When numerical modifiers such as K or M are used, they refer to binary rather than decimal form. Thus, for example, 1 KByte would be equivalent to 1024, not 1,000 bytes.

NOTICES

Additional information may be obtained from:

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High Performance, Highly integrated 2D/3D Graphics and Video Accelerator

- 135 MHz integrated DAC
- Three PLLs integrated on chip
- 64-bit 2D/3D Graphics Engine
- Integrated NTSC/PAL TV encoder
- 1-cycle linear addressing of the memory space facilitates high performance device drivers

Emerging Bus Architecture Integrated Interface

- Base line 66 MHz AGP support
- Glueless PCI 2.1 interface
- PCI bus mastering for display list processing and video capture support

High Performance, Flexible Memory Support

- 83 MHz SGRAM/SDRAM
- 66 MHz 1-cycle EDO DRAM
- 2 MB and 4 MB Support:
  - Two (2 MB) or four (4MB) 256Kx32 SGRAMs
  - Two (4 MB) 512Kx32 SGRAMs
  - Four (2 MB) or eight (4MB) 256Kx16 SDRAMs
  - Four (2MB) or eight (4 MB) 256Kx16 EDO DRAMs
  - Two (4 MB) 512Kx32 EDO DRAMs
  - Two (2 MB) or four (4MB) 256Kx32 EDO DRAMs

Full Featured, High Performance S3d™ Engine

- Flat and Gouraud shading for 3D images
- High quality 3D texture mapping
- Perspective correction
- Bi-linear and tri-linear texture filtering
- MIP-mapping
- Depth cueing, fogging and alpha blending

- Video texture mapping
- Z-buffering
- High performance 2D acceleration

Direct Interface to State of the Art Flat Panel Displays

- Support for VGA and SVGA active matrix TFT flat panel displays with 9, 12, 18, 24-bit interface (1 pixel/clock)
- Support for XGA and SXGA active matrix TFT flat panel displays with 2x9, 2x12, 2x18-bit interface (2 pixels/clock)
- Support for passive matrix DSTN flat panel displays up to XGA resolution with 16- or 24-bit interface
- Support for passive matrix SSTN flat panel displays with 8, 16 or 24-bit interfaces
- Advanced frame rate control (FRC) for STN panels
- 2x2 and 4x4 dithering algorithms providing up to 16 million colors for TFT panels and 14 million colors for STN panels
- Panel data polarity switching for EMI reduction
- Auto-expansion and centering for text and graphics modes on high resolution panels
- Supports LVDS or PanelLink™ high speed serial transmitters externally. This allows support for up to 24 bits/pixel XGA TFT panels at 1 pixel/clock.

Industry Leading DuoView™ Simultaneous Display Capability

- Simultaneous CRT, flat panel or TV display (or any combination thereof)
- Two independent images on CRT, flat panel or TV
- Separate and optimized refresh rates for flat panel and CRT utilizing the DuoView functionality

Comprehensive Power Management

- S3® dynamic power management yields low power normal operation
- Low power Standby and Suspend modes
- Self-refresh and slow-refresh DRAM support
- Hardware and software mechanisms to enter Suspend mode
- PCI power management

Industry-Standard Streams Processor Video Acceleration

- Supports separate graphics and video (primary and secondary) streams to enable different video and graphics pixel depths for higher bandwidth and better memory management
- Dynamic stretching and blending of graphics and video streams
- High quality video playback of MPEG-2 video steam with vertical and horizontal interpolation
- Brightness, hue and saturation control through register bits enables software controlled adjustments to display devices
- Support for Cinepak™, Indeo™ and other MPEG-1 video sources

Integrated TV Encoder

- Direct output to NTSC/PAL TV monitors
- Composite or S-Video format
- 3-line flicker filter ensures excellent TV output quality
- Underscan compensation to display VGA modes on NTSC TV

Fully compliant ZV-Port interface with Device Driver Support for VPM

Glueless 8 or 16-bit interface to Video Digitizers

Big Endian and little Endian Byte Ordering Support

Entire I/O address Space Can be Memory Mapped

Two (2) Programmable Pulse Width Modulated (PWM) Outputs to Provide Contrast and Brightness Adjustment, Thereby Reducing External Components

256 Pin BGA Package

1.1 INTRODUCTION

The ViRG®/MX dual image graphics video accelerators introduce a new class of performance to notebook computers and other portable applications utilizing flat panel displays.

1.2 HIGH PERFORMANCE FEATURES

ViRGE/MX includes a number of unique features to enhance the graphics performance:

- 66 MHz Base Line AGP Support
- 33 MHz PCI Master/Slave interface
- 1-cycle linear addressing of the memory space
- 83 MHz synchronous memory interface
- 64x64x2 Hardware pop-up icon
- 66 MHz MCLK for EDO memories and 83 MHz MCLK for SGRAM/SDRAM interface
- 135 MHz DCLK for high resolution high refresh mode support

1.3 AGP SUPPORT

ViRGE/MX provides entry level support for the emerging Accelerated Graphics Port (AGP) initiative which, when working cooperatively with the S3d engine provides enhanced 3D graphics performance. The AGP interface provides a high bandwidth, low latency connection to system memory, thereby improving the performance of 2D and 3D graphics applications.

1.4 S3d ENGINE

The S3d engine is derived from the ViRGE family of high performance desktop graphics controllers. The enhanced S3d engine provides excellent 2D graphics performance and a full-featured high performance 3D rendering engine for realistic 3D experience for all 3D applications. Following are the S3d engine features:

- Flat and Gouraud shading for 3D applications
- High quality 3D texture mapping
- Perspective correction
- Bi-linear and tri-linear texture filtering
- MIP-mapping
- Depth cueing and fogging
- Z-buffering
- Alpha blending
- Video texture mapping
- Excellent 2D graphics performance

1.5 DISPLAY INTERFACE

ViRGE/MX supports a wide range of existing and newly defined panel interfaces and types. ViRGE/MX supports active and passive matrix technology flat panel displays with varying color depths and pixel interfaces. The following is a summary of the panel support:

- Support for VGA and SVGA active matrix TFT flat panel displays with 9, 12, 18, 24-bit interface (1 pixel/clock)
- Support for XGA and SXGA active matrix TFT flat panel displays with 2x9, 2x12, 2x18-bit interface (2 pixels/clock)
- Support for passive matrix DSTN flat panel displays up to XGA resolution with 16- or 24-bit interface
- Support for passive matrix SSTN flat panel displays with 8, 16 or 24-bit interfaces
- Advanced frame rate control (FRC) for STN panels
- 2x2 and 4x4 dithering algorithms providing up to 16 million colors for TFT panels and 14 million colors for STN panels
- Panel data polarity switching for EMI reduction
- Auto-expansion and centering for text and graphics modes on high resolution panels
- Supports LVDS or PanelLink™ high speed serial transmitters externally. This allows support for up to 24 bits/pixel XGA TFT panels at 1 pixel/clock.
- Advanced power sequencing techniques for the panel power and control/data signals
- Two register programmable pulse width modulation outputs to adjust the flat panel brightness and contrast

1.6 HIGH-PERFORMANCE FLEXIBLE MEMORY SUPPORT

ViRGE/MX supports a 2MB or 4MB video frame buffer with either EDO DRAM, synchronous DRAM (SDRAM) or synchronous graphics RAM (SGRAM). Memory clock (MCLK) rates of 83 MHz for SGRAM/SDRAM and 66 MHz for EDO DRAM (1-cycle operation) are supported at 3.3V memory interface operation.

ViRGE/MX supports memory component configurations of 256Kx16, 256Kx32, and 512Kx32 for EDO DRAM and SGRAM/SDRAM. Video frame buffer sizes of 2MB and 4MB are supported.

1.7 TV OUTPUT

All display modes supported by VirGE/MX and Streams Processor hardware video overlay can be directly output to a television monitor (NTSC or PAL). ViRGE/MX has a dedicated DAC and output pins distinct from the RGB monitor output. No external analog MUX or buffer is required to isolate TV and RGB monitor inputs, saving cost and board space. S3's DuoView architecture provides the added benefit of simultaneous TV/LCD display for presentation or gaming applications. Either composite or S-Video output are provided.

All display modes are supported with TV output. The integrated encoder performs non-interlaced to interlaced timing conversion for all text and graphics modes.

The programmable TV pixel clock rate for NTSC or PAL is generated from the 14.31818 MHz clock reference or from an optional 27 MHz clock reference. Use of a high accuracy (50-100 ppm) external oscillator reference is recommended.

ViRGE/MX employs a 3-line flicker filter with adjustable weighting to substantially reduce flicker on TV monitors while maintaining a sharp image for text and fine graphics. Adaptive filtering based on flicker component (vertical pixel differential) is implemented using the Set Interpolative Threshold (SIT) method. This method looks at the difference of the primary Y value and the Y value of the vertically adjacent pixel. If the Y difference is larger or equal to the SIT value (set via register entry) then a filtering fraction (also set via register entry) is applied, otherwise if the Y difference is less than the SIT value then no filtering is applied. The result is a highly flexible weighted filtering for optimum image quality.

Vertical underscanning support is provided for 480-line VGA modes.

1.8 DuoView DISPLAY

ViRGE/MX builds on S3's DuoView architecture, taking advantage of the bandwidth offered by SGRAM and the flexibility provided by having two completely independent clock synthesizers for the two display control channels.

ViRGE/MX has two CRT controllers; Controller 1 and Controller 2. Either can be used to drive a CRT, either can be used to drive a flat panel, and either can be used to drive a TV. The Streams Processor can be used with either controller. Controller 2 can only be used to display Enhanced modes, while Controller 1 can be used to display any standard VGA mode as well as Enhanced modes. Additionally, Controller 1 contains logic for hardware centering and expansion for LCDs, while Controller 2 does not.

The DCLK rate used by each controller path can be individually specified. This provides a tremendous degree of flexibility, including the ability to have completely different timings on the two displays. Therefore, the refresh rate for each display can be independently optimized and a non-interlaced LCD can be driven simultaneously with an interlaced CRT or TV. ViRGE/MX's independent analog RGB and TV outputs even provide the ability to drive 3 displays simultaneously: TV, CRT, and LCD, for ultimate flexibility in presentation or gaming applications.

In simultaneous display mode, only one controller is used to drive both the CRT and the LCD. Simultaneous display means that the same image is shown to both display devices with the same timings. Video output using the Streams Processor is displayed on both screens, as are the hardware cursor and hardware icon.

In DuoView modes, both CRT controller paths are active. Each path can drive any of the display outputs. Therefore the choice of which path controls which output is a matter of which display device may need hardware compensation for centering and expansion and thus require Controller 1.

1.9 STREAMS PROCESSOR VIDEO ACCELERATION

The S3 Streams Processor processes data from the graphics frame buffer, composes it and outputs the results to the internal display controllers for display on LCD, CRT, and TV.

The processor can compose data from up to 4 independent streams:

1. Primary Stream - RGB graphics data

2. Secondary Stream = RGB or YUV/YCbCr (video) data from another region within the frame buffer.
3. Hardware Icon - 64x64x4 or 128x128x2
4. Hardware Cursor - 64x64x2 cursor

Regardless of the input formats, the Streams processor creates a composite RGB-24 (8,8,8) output to the DACs. This means that, for example, RGB-8 pseudo-color graphics data can be overlaid with true-color-equivalent (24-bit/pixel) video data. The result is improved video quality and/or reduced memory bandwidth requirements as compared with systems that require both graphics and video data to be stored in the same frame buffer format.

ViRGE/MX enables both horizontal and vertical interpolation of the secondary stream overlay. Integrated line buffers allow vertical interpolation of MPEG-2 (720x480) video source data. The Streams Processor performs overlay via either color key or chroma key for flexible blending of video overlays with graphics backgrounds.

1.10 FULLY COMPLIANT ZV-PORT SUPPORT WITH VPM DEVICE DRIVERS

The ViRGE/MX Local Peripheral Bus (LPB) is fully compliant with the ZV-Port specification. The LPB provides the following interfaces:

- ZV-Port
- Industry standard video digitizers (8-bit or 16-bit interfaces). Registers are programmed via a serial I^2C interface.
- Host Video Data Pass-through. This allows decimation of 32-bit CPU data being written to the frame buffer.

Full Video Port Manager (VPM) version 1.10 device driver support is provided for MPEG-1 and live video PCCARDs under Windows 95 and Windows 3.1. VPM device drivers will be developed for MPEG-2 PCCARD's as they become commercially available.

Section 2: Mechanical Data

2.1 THERMAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
Thermal Resistance Θ_{JC}		5		°C/W
Thermal Resistance Θ_{JA} (Still Air)		22.3		°C/W
Junction Temperature			125	°C
Case Temperature			123	°C

2.2 MECHANICAL DIMENSIONS

The mechanical dimensions for the 256-pin BGA package are given in Figure 2-1.

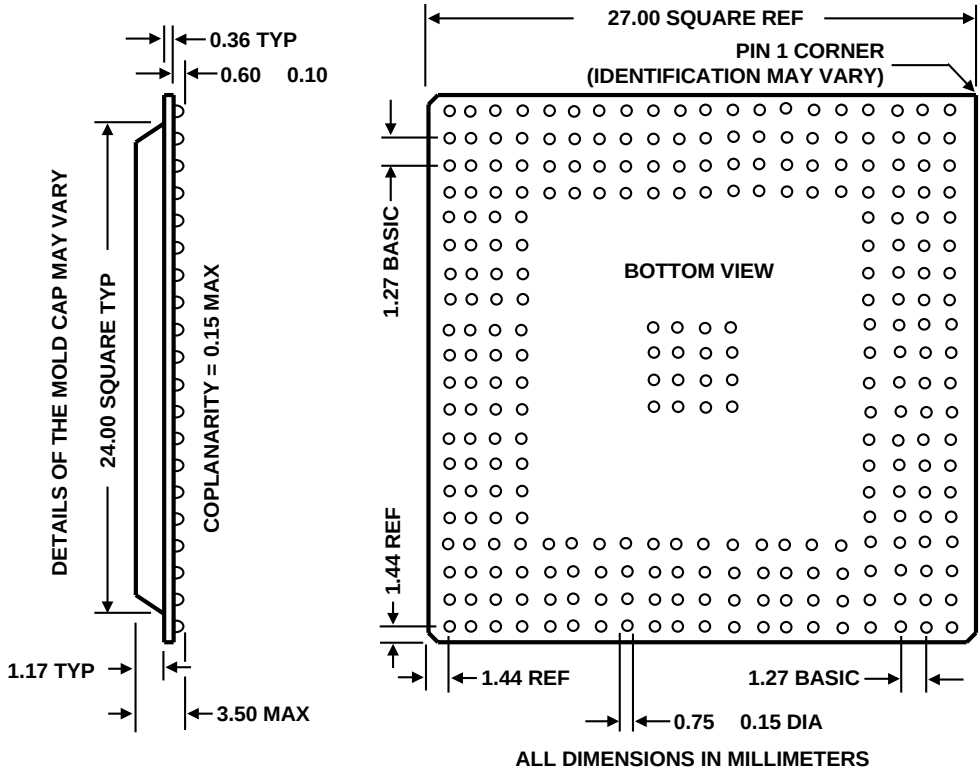


Figure 2-1. 256-pin BGA Mechanical Dimensions

Section 3: Pins

3.1 PINOUT DIAGRAMS

ViRGE/MX comes in a 256-pin BGA package . The pinout is shown in Figure 3-1.

A1 XOUT	A2 ENAVDD	A3 FPVSYNC FLM	A4 FPD1	A5 FPD4	A6 FPD8	A7 FPD11	A8 FPD15	A9 FPD18	A10 FPD21	A11 FPD24	A12 PPD28	A13 FPD31	A14 FPD35	A15 PD63	A16 PD60	A17 PD57	A18 PD56	A19 PD43	A20 PD42
B1 CLKAVDD 1	B2 XIN/ EDCLK1	B3 FPSCLK	B4 FPD0	B5 FPD3	B6 FPD7	B7 FPD10	B8 FPD14	B9 FPD17	B10 FPD20	B11 FPD23	B12 FPD27	B13 FPD30	B14 FPD34	B15 FPDE/ MOD	B16 PD61	B17 PD58	B18 PD47	B19 PD44	B20 PD41
C1 VREF	C2 CLKAVSS1	C3 ENAVEE	C4 FPHSYNC LP	C5 FPD2	C6 FPD6	C7 FPD9	C8 FPD13	C9 FPD16	C10 FPD19	C11 FPD22	C12 FPD26	C13 FPD29	C14 FPD33	C15 FPPOL/ ROMEN	C16 PD62	C17 PD59	C18 PD46	C19 PD45	C20 PD40
D1 RSET	D2 AVSS	D3 CLKAVDD 2	D4 STWR/ GOP0	D5 VDDFPI	D6 FPD5	D7 VSSSUB	D8 FPD12	D9 VDDCORE	D10 PWM0	D11 VSSCORE	D12 FPD25	D13 VDDFPI	D14 FPD32	D15 FPGPIO	D16 VDDCORE	D17 PD33	D18 PD34	D19 PD55	D20 PD48
E1 AR	E2 AVSS	E3 COMP	E4 CLKAVSS2													E17 PD32	E18 PD35	E19 PD54	E20 PD49
F1 AVDD	F2 AG	F3 AB	F4 AY													F17 VDDMEM5	F18 PD36	F19 PD53	F20 PD50
G1 TVDAC VDD	G2 AC	G3 TVDAC VSS	G4 CLKAVSS3													G17 VDDMEM	G18 PD37	G19 PD52	G20 PD51
H1 HSYNC	H2 VSYNC	H3 LD0	H4 VDDLPB5													H17 CS0	H18 PD38	H19 PD39	H20 CAS4/ DQM4
J1 LD1	J2 LD2	J3 LD3	J4 VDDLPB					J9 VSSPAD2	J10 VSSPAD2	J11 VSSPAD2	J12 VSSPAD2					J17 WE	J18 CAS6/ DQM6	J19 CAS5/ DQM5	J20 SDCLKI
K1 VREQ/ HREF	K2 LD4	K3 LD5	K4 VSSCORE					K9 VSSPAD1	K10 VSSPAD2	K11 VSSPAD2	K12 VSSPAD2					K17 RAS0/CS1 MA10	K18 CAS7/ DQM7	K19 OE/ SDCAS	K20 SDCLK
L1 CREQ/ VS	L2 LD6	L3 LD7	L4 VDDCORE					L9 VSSPAD1	M10 VSSPAD1	L11 VSSPAD2	L12 VSSPAD2					L17 RAS1/ SDRAS	L18 MA8	L19 MA7	L20 MA0
M1 LCLK/ VCLK	M2 SPCLK	M3 SPDAT	M4 PWM1/ ODD					M9 VSSPAD1	M10 VSSPAD1	M11 VSSPAD1	M12 VSSPAD1					M17 MA9	M18 MA2	M19 MA6	M20 MA1
N1 LPBEN/ EMCLK	N2 LD8	N3 LD9	N4 EDCLK2													N17 VDDMEM	N18 MA5	N19 MA4	N20 MA3
P1 LD10	P2 PD11	P3 LD12	P4 LD13													P17 VSSCORE	P18 PD26	P19 PD13/ RA13	P20 PD8/ RA8
R1 LD14	R2 LD15	R3 RESET	R4 REQ													R17 DSF	R18 PD27	R19 PD14/ RA14	R20 PD9/ RA9
T1 CLK32	T2 STANDBY	T3 SUSPEND	T4 VDDSYS													T17 PD31	T18 PD28	T19 PD15/ RA15	T20 PD10/ RA10
U1 SCLK	U2 INTA	U3 AD25	U4 AD23	U5 GNT	U6 VDDSYS	U7 VDDSYS5	U8 STOP	U9 AD14	U10 VSSCORE	U11 N/C	U12 N/C	U13 CLKRUN	U14 CAS0/ DQM0	U15 SDCLKEN	U16 VDDCORE	U17 PD0/ RA0	U18 PD29	U19 PD24	U20 PD11/ RA11
V1 AD31	V2 AD29	V3 C/BE3	V4 AD21	V5 AD18	V6 AD16	V7 IRDY	V8 PAR	V9 AD12	V10 AD9	V11 AD7	V12 AD4	V13 AD1	V14 CAS1/ DQM1	V15 PD7/ RA7	V16 PD2/ RA2	V17 PD1/ RA1	V18 PD30	V19 PD25	V20 PD12/ RA12
W1 AD30	W2 AD28	W3 AD24	W4 AD22	W5 AD19	W6 FRAME	W7 DEVSEL	W8 AD15	W9 AD13	W10 AD10	W11 C/BE0	W12 AD5	W13 AD2	W14 CAS2/ DQM2	W15 PD6/ RA6	W16 PD3/ RA3	W17 PD23/ RD7	W18 PD22/ RD6	W19 PD21/ RD5	W20 PD20/ RD4
Y1 AD27	Y2 AD26	Y3 IDSEL	Y4 AD20	Y5 AD17	Y6 C/BE2	Y7 TRDY	Y8 C/BE1	Y9 AD11	Y10 AD8	Y11 AD6	Y12 AD3	Y13 AD0	Y14 CAS3/ DQM3	Y15 PD5/ RA5	Y16 PD4/ RA4	Y17 PD19/ RD3	Y18 PD18/ RD2	Y19 PD17/ RD1	Y20 PD16/ RD0

Figure 3-1. Pinout (Top View)

3.2 PIN DESCRIPTIONS

The following table provides a brief description of each pin. Where two drive levels are given, the value is programmable. The following abbreviations are used for pin types. ’

I - Input signal
O - Output signal
B - Bidirectional signal

Table 3-1. Pin Descriptions

Symbol	Type	Drive (mA)	Description
PCI BUS INTERFACE (All pins use VDDSYS)			
AD[31:0]	B	8/16	Multiplexed Address/Data Bus. A bus transaction (cycle) consists of an address phase followed by one or more data phases. SRA_7 controls the drive.
C/BE[3:0]	B	24	Bus Command/Data Byte Enables. These signals carry the bus command during the address phase and the byte enables during the data phase.
SCLK	I		PCI System Clock.
INTA	O	4	Interrupt Request.
IRDY	B	24	Initiator Ready. This signal is an input when an external bus master has control of the PCI Bus and an output for bus master PCI operation.
TRDY	B	24	Target Ready. This signal is an output when an external bus master has control of the PCI Bus and an input for bus master PCI operation.
DEVSEL	B	24	Device Select. This signal is an output when an external bus master has control of the PCI Bus and an input for bus master PCI operation.
IDSEL	I		Initialization Device Select. This input is the chip select for PCI configuration register reads/writes.
RESET	I		System Reset. Asserting this signal forces the registers and state machines to a known state.
FRAME	B	24	Cycle Frame. This signal is an input when an external bus master has control of the PCI Bus and an output for bus master PCI operation.
PAR	B	24	Parity. This signal is an output from the bus master during writes and an input to the bus master during reads.
STOP	B	24	Stop. This signal is an input to the bus master from the target indicating a request to stop the current transaction.
REQ	O	4	Request. This signal is asserted request control of the PCI Bus for bus master DMA operation.
GNT	I		Grant. Assertion of this signal grants control of the PCI Bus for bus master DMA operation.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type/ Drive	Drive (mA)	Description
DISPLAY MEMORY INTERFACE (All pins use VDDMEM)			
Address and Data			
MA[10:0]	O	4/8	Memory Address Bus. The video memory row and column addresses are multiplexed on these lines. MA9 and MA10 are the bank select pins for 256Kx and 512Kx synchronous memories respectively. CR77_3 controls the drive.
PD[63:0]	B	4/8	Display Memory Pixel Data Bus Lines 63:0. PD[31:0] are also used as the system configuration strapping bits, providing system configuration and setup information upon power-on reset. See Section 5 for a description of this function. CR77_2 controls the drive.
DRAM Memory Control			
$\overline{\text{RAS}}$[1:0]	O	8	Row Address Strobes.
$\overline{\text{CAS}}$[7:0]	O	8	Column Address Strobe Lines 7:0.
$\overline{\text{WE}}$	O	16	Write Enable.
$\overline{\text{OE}}$	O	16	Output Enable.
SGRAM/SDRAM Memory Control			
SDCLK	O	16/8	SGRAM/SDRAM Clock. CR77_1 controls the drive.
SDCLKI	I		Return SDCLK.
SDCLKEN	O	8	SGRAM/SDRAM Clock Enable.
$\overline{\text{SDRAS}}$	O	8	SDRAM Row Address Strobe.
$\overline{\text{SDCAS}}$	O	16	SDRAM Column Address Strobe.
DQM[7:0]	O	8	SGRAM/SDRAM Data Input/Output Masks.
$\overline{\text{CS}}$[1:0]	O	8	SGRAM/SDRAM Chip Selects. $\overline{\text{CS0}}$ selects the first two MBytes and $\overline{\text{CS1}}$ selects the second two MBytes.
$\overline{\text{WE}}$	O	16	SGRAM/SDRAM Write Enable.
$\overline{\text{DSF}}$	O	8	SGRAM Special Function.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Drive (mA)	Description
CRT/TV VIDEO INTERFACE (All pins use AVDD except as noted)			
COMP			Compensation. This pin is tied to VDD through a 0.1 µF capacitor.
VREF			Voltage Reference. This pin is tied to VSS through a 0.1 µF capacitor.
RSET			Reference Resistor. This pin is tied to VSS through an external resistor to control the full-scale current value.
AR	O		Analog Red. Analog red output to the CRT monitor.
AB	O		Analog Blue. Analog blue output to the CRT monitor.
AG	O		Analog Green. Analog green output to the CRT monitor.
AY	O		Analog Luminance. Output to TV monitor.
AC	O		Analog Chromanance. Output to TV monitor.
HSYNC	O		Horizontal Sync. Output to CRT.
VSYNC	O		Vertical Sync. Output to CRT.
FLAT PANEL INTERFACE (All pins use VDDFPI except as noted)			
FPD[35:0]	O	16/8	Flat Panel Data. The meanings of these outputs vary depending on the type of panel. See Section 11 for tables listing all output combinations.
FPDE/ MOD	O	16/8	Flat Panel Display Enable/AC Modulation Signal. When a TFT panel is being driven, this is the display enable signal. When an STN panel is being driven, this is by default the display enable signal, which is not normally used but may be required for external panel control. If SR34_7 = 1, this is the AC modulation signal for those panels that require it.
FPSCLK	O	8	Flat Panel Shift Clock. This is the shift (dot) clock for LCD panels.
FPGPIO	B	8	Flat Panel General Purpose I/O. This pin functions as a general purpose I/O pin, outputs one of the internally generated clocks or indicates the panel on status, depending on the setting of SR35_2-0.
FPHSYNC/LP	O	16/8	Flat Panel HSYNC. This is the HSYNC signal for TFT panels and the LP (line pulse or new line start) signal for STN panels.
FPVSYNC/FLM	O	16/8	Flat Panel VSYNC. This is the VSYNC signal for TFT panels and the FLM (first line marker or new frame start) signal for STN panels.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Drive (mA)	Description
FPPOL	O	16/8	Flat Panel Polarity. If CR6F_0 = 1, this signal tells the panel that the polarity of the data is reversed, thereby minimizing the number of data lines switching in each cycle. This is used in a few highly advanced panels. If CR6F_0 = 0, this is the BIOS ROM enable output.
PWM[1:0]	O	4	Pulse Width Modulation. (PWM1 - VDDLPB). The PWM1 function is selected (versus ODD) when SR52_7 = 1.
FLAT PANEL POWER CONTROL (All pins use VDDFPI)			
ENAVDD	O	4	Enable VDD. This signal is driven high to external logic to initiate a flat panel power up sequence. It is driven low a programmable time (SR41_2) after the panel control signals and ENAVEE are driven low in Standby or Suspend Mode or if the flat panel is shut off via SR31_4.
ENAVEE	O	4	Enable VEE. This signal is driven high a programmable time (SR41_3) after ENAVDD is driven high during a flat panel power up sequence. This signals external logic to turn on the bias voltage to the flat panel. It is driven low for Standby or Suspend Mode or if the flat panel is shut off via SR40_4. This signals external logic to turn off the bias voltage to the flat panel.
STANDBY	I		Standby. If SR44_4 = 0, driving the STANDBY pin high initiates Standby mode and driving it low initiates exiting of Standby. If SR44_4 = 1, the system is always trying to go into Standby mode and 4 SCLK high pulses on the STANDBY pin either prevent this or take the system out of Standby, resetting the timer in either case.
SUSPEND	I		Suspend. A low to high transition initiates a Suspend mode sequence and a high to low sequence initiates exiting from Suspend mode.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Drive (mA)	Description
CLOCK CONTROL AND INPUT (Power individually noted)			
XIN	I		Reference Frequency Input. If an external 14.318 MHz crystal is used, it is connected between XOUT and this pin. Connection of a high accuracy (50 - 100 ppm) external oscillator to this pin is recommended. If this is done, the input must be the same voltage as AVDD. (AVDD)
XOUT	O		Crystal Output. This pin drives the crystal via an internal oscillator. (AVDD)
EMCLK	I		External MCLK. If PD11 is strapped low at power-on, pin N1 becomes the MCLK input, bypassing the internal oscillator. This function can also be enabled by setting SR14_6 to 1. (VDDLPB)
EDCLK[1:2]	I		External DCLKs. If PD11 is strapped low at power-on, pin B2 becomes the DCLK1 input and pin N4 becomes the DCLK2 input, both bypassing the internal oscillators. The DCLK1 input function can also be enabled by setting SR14_7 to 1. The DCLK2 input function can also be enabled by setting SRB_7 to 1. The latter can be used directly or as a reference frequency for the DCLK2 PLL depending on the setting of SRB_5. (EDCLK1 - AVDD, EDCLK2 - VDDLPB)
CLK32	I		32 kHz Clock. An external TTL 32 kHz source is connected to this pin. It is used for panel power sequencing and video memory refresh when in Suspend mode. During Standby and Suspend, this signal is output on HSYNC and VSYNC for default register settings. See description for SR42_0. (VDDSYS)
$\overline{\text{CLKRUN}}$	B	24	Clock Run. PCI power management clock control pin. A central resource drives this pin high to signal ViRGE/MX to turn off its clocks. ViRGE/MX asserts this signal if it is unable to do so at the time of the request. This line is pulled up externally. (VDDSYS)

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Drive (mA)	Description
MISCELLANEOUS FUNCTIONS (Power individually noted)			
$\overline{\text{ROMEN}}$	O	4	ROM Enable. This signal provides the chip output enable input for BIOS ROM reads. It is multiplexed with the FPPOL signal and is selected when CR6F_0 = 0. (VDDMEM)
RA[15:0}	O	4	ROM Address Bus. These signals are multiplexed on PD lines. If a video BIOS is used, it must be immediately shadowed after boot. (VDDMEM)
RD[7:0]	I		ROM Data Bus. These signals are multiplexed on PD lines. If a video BIOS is used, it must be immediately shadowed after boot. (VDDMEM)
$\overline{\text{STWR}}$	O	4	Strobe Write. If SR1A_4 is set to 1, pin D4 acts as STWR. This signal is asserted whenever a write is made to CR5C. It is used to enable a General Output Port latch. MCLK is output instead of this signal if SR15_2 = 1. MCLK output is used only for test purposes. (VDDFPI)
GOP0	O	4	General Output Port. When SR1A_4 is cleared to 0, pin C3 acts as GOP0. The content of CR5C_0 is reflected on this pin when this bit is programmed. (VDDFPI)
SPCLK	B	8	Serial Port Clock. This is the clock for serial data transfer, either for I^2C or DDC2 monitor data communications. As an output, it is programmed via MMFF20_0. As an input, its status is read via MMFF20_2. In either case the serial port must be enabled by setting MMFF20_4 to 1. PD[26:25] can be strapped to allow I/O (E2H or E8H) port access to the Serial Port register while ViRGE/MX is disabled. (VDDLPB)
SPDAT	B	8	Serial Port Data. This is the data signal for serial data transfer, either for I^2C or DDC2 monitor data communications. As an output, it is programmed via MMFF20_1. As an input, its status is read via MMFF20_3. In either case the serial port must be enabled by setting MMFF20_4 to 1. PD[26:25] can be strapped to allow I/O (E2H or E8H) port access to the Serial Port register while ViRGE/MX is disabled. (VDDLPB)
LPBEN	O	4	LPB Device Enable. This signal is connected to an external video source to enable input. The output level is controlled via SRD_0.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Drive (mA)	Description
ZV-PORT (All pins use VDDLPB)			
LD[15:0]	I		Data. YUV input from PC Card
LCLK	I		Clock. PCLK input from PC Card
HREF	I		HSYNC. HREF input from PC Card
VS	I		VSYNC. VSYNC input from PC Card
SCENIC HIGHWAY (All pins use VDDLPB)			
Bidirectional Mode			
LD[7:0]	B	4	LPB Data.
LCLK	I		LPB Clock.
$\overline{\text{VREQ}}$/VRDY	O	4	Video Request/Ready.
$\overline{\text{CREQ}}$/CRDY	I		Decoder Request/Ready.
Video 8 and 16 Modes			
LD[15:0]	I		LPB Data Bus [15:0]. Video data input. LD[7:0] are used for 8-bit interfaces.
HREF	I		HSYNC.
VS	I		VSYNC.
$\overline{\text{ODD}}$	I		ODD/EVEN field. High = even field input from the digitizer. Low = odd field input. This function is selected (versus the PWM1 function) when SR52_=1.
POWER AND GROUND			
VDDCORE	I		Digital power supply to the core logic
VDDCRT	I		Digital power supply to the CRT block pads
VDDFPI	I		Digital power supply to the flat panel block pads
VDDLPB	I		Digital power supply to the LPB block pads
VDDLPB5	I		5V tolerance for LPB interface
VDDMEM	I		Digital power supply to the memory subsystem pads
VDDMEM5	I		5V tolerance for memory interface
VDDSYS	I		Digital power supply to the system bus interface pads
VDDSYS5	I		5V tolerance for system bus interface
CLKAVDD[1:2]	I		Analog power supply (1 = DCLK synthesizers, 2 = MCLK synthesizer). This must be the same voltage as VDDCORE
TVDACVDD	I		Analog power for TV DAC
AVDD	I		Analog power
VSSPAD	I		Digital ground
VSSCORE	I		Digital ground (core)
VSSSUB	I		Digital ground (substrate)
AVSS	I		Analog ground
CLKAVSS[1:3]	I		Analog ground for PLLs

3.3 PIN LISTS

Table 3-2 lists all pins alphabetically. Table 3-3 lists all pins in numerical order.

Table 3-2. Alphabetical Pin Listing

Name	PIN(S)
AB	F3
AC	G2
AD[31:16]	V1, W1, V2, W2, Y1, Y2, U3, W3, U4, W4, V4, Y4, W5, V5, Y5, V6,
AD[15:0]	W8, U9, W9, V9, Y9, W10, V10, Y10, V11, Y11, W12, V12, Y12, W13, V13, Y13
AG	F2
AR	E1
AVDD	F1
AVSS	D2, E2
AY	F4
$\overline{\text{CAS}}$[7:0]	K18, J18, J19, H20, Y14, W14, V14, U14
$\overline{\text{C/BE}}$[3:0]	V3, Y6, Y8, W11
CLK32	T1
CLKAVDD[1:2]	B1, D3
CLKAVSS[1:3]	C2, E4, G4
$\overline{\text{CLKRUN}}$	U13
COMP	E3
$\overline{\text{CREQ}}$/CRDY	L1
$\overline{\text{CS}}$[1:0]	K17, H17
$\overline{\text{DEVSEL}}$	W7
DQM[7:0]	K18, J18, J19, H20, Y14, W14, V14, U14
DSF	R17
EDCLK[1:2]	B2, N4
EMCLK	N1
ENAVDD	A2
ENAVEE	C3
FLM	A3
FPD[35:27]	A14, B14, C14, D14, A13, B13, C13, A12, B12,
FPD[26:18]	C12, D12, A11, B11, C11, A10, B10, C10, A9,
FPD[17:9]	B9, C9, A8, B8, C8, D8, A7, B7, C7,
FPD[8:0]	A6, B6, C6, D6, A5, B5, C5, A4, B4
FPDE	B15
FPGPIO	D15
FPHSYNC	C4
FPPOL	C15
FPSCLK	B3
FPVSYNC	A3
$\overline{\text{FRAME}}$	W6

Table 3-2. Alphabetical Pin Listing (Continued)

Name	PIN(S)
$\overline{\text{GNT}}$	U5
GOP0	D4
HREF	K1
HSYNC	H1
IDSEL	Y3
$\overline{\text{INTA}}$	U2
$\overline{\text{IRDY}}$	V7
LCLK	M1
LD[15:0]	R2, R1, P4, P3, P2, P1, N3, N2, L3, L2, K3, K2, J3, J2, J1, H3
LP	C4
LPBEN	N1
MA[10:0]	K17, M17, L18, L19, M19, N18, N19, N20, M18, M20, L20
MOD	B15
NO CONNECT	U11, U12
$\overline{\text{ODD}}$	M4
$\overline{\text{OE}}$	K19
PAR	V8
PD[63:48]	A15, C16, B16, A16, C17, B17, A17, A18, D19, E19, F19, G19, G20, F20, E20, D20
PD[47:32]	B18, C18, C19, B19, A19, A20, B20, C20, H19, H18, G18, F18, E18, D18, D17, E17
PD[31:16]	T17, V18, U18, T18, R18, P18, V19, U19, W17, W18, W19, W20, Y17, Y18, Y19, Y20
PD[15:0]	T19, R19, P19, V20, U20, T20, R20, P20, V15, W15, Y15, Y16, W16, V16, V17, U17
PWM[1:0]	M4, D10
RA[15:0]	T19, R19, P19, V20, U20, T20, R20, P20, V15, W15, Y15, Y16, W16, V16, V17, U17
$\overline{\text{RAS}}$[1:0]	L17, K17
RD[7:0]	W17, W18, W19, W20, Y17, Y18, Y19, Y20
$\overline{\text{REQ}}$	R4
$\overline{\text{RESET}}$	R3
$\overline{\text{ROMEN}}$	C15
RSET	D1
SCLK	U1
$\overline{\text{SDCAS}}$	K19
SDCLK	K20
SDCLKEN	U15
SDCLKI	J20
$\overline{\text{SDRAS}}$	L17
SPCLK	M2
SPDAT	M3
STANDBY	T2
$\overline{\text{STOP}}$	U8
$\overline{\text{STWR}}$	D4
SUSPEND	T3
$\overline{\text{TRDY}}$	Y7

Table 3-2. Alphabetical Pin Listing (Continued)

Name	PIN(S)
TVDACVDD	G1
TVDACVSS	G3
VCLK	M1
VDDCORE	D9, D16, L4, U16
VDDFPI	D5, D13
VDDLPB	J4
VDDLPB5	H4
VDDMEM	G17, N17
VDDMEM5	F17
VDDSYS	T4, U6
VDDSYS5	U7
VREF	C1
$\overline{\text{VREQ}}$/VRDY	K1
VS	L1
VSSCORE	D11, K4, P17, U10
VSSPAD1	K9, L9, L10, M9, M10, M11, M12
VSSPAD2	J9, J10, J11, J12, K10, K11, K12, L9, L10, L11, L12
VSSSUB	D7
VSYNC	H2
$\overline{\text{WE}}$	J17
XIN	B2
XOUT	A1

Table 3-3. Numerical Pin Listing

Number	Name	Number	Name
A1	XOUT	C3	ENAVEE
A2	ENAVDD	C4	FPHSYNC/LP
A3	FPVSYNC/FLM	C5	FPD2
A4	FPD1	C6	FPD6
A5	FPD4	C7	FPD9
A6	FPD8	C8	FPD13
A7	FPD11	C9	FPD16
A8	FPD15	C10	FPD19
A9	FPD18	C11	FPD22
A10	FPD21	C12	FPD26
A11	FPD24	C13	FPD29
A12	FPD28	C14	FPD33
A13	FPD31	C15	FPPOL/$\overline{\text{ROMEN}}$
A14	FPD35	C16	PD62
A15	PD63	C17	PD59
A16	PD60	C18	PD46
A17	PD57	C19	PD45
A18	PD56	C20	PD40
A19	PD43	D1	RSET
A20	PD42	**D2**	**AVSS**
B1	**CLKAVDD1**	**D3**	**CLKAVDD2**
B2	XIN/EDCLK1	D4	$\overline{\text{STWR}}$/GOP0
B3	FPSCLK	**D5**	**VDDFPI**
B4	FPD0	D6	FPD5
B5	FPD3	**D7**	**VSSSUB**
B6	FPD7	D8	FPD12
B7	FPD10	**D9**	**VDDCORE**
B8	FPD14	D10	PWM0
B9	FPD17	**D11**	**VSSCORE**
B10	FPD20	D12	FPD25
B11	FPD23	**D13**	**VDDFPI**
B12	FPD27	D14	FPD32
B13	FPD30	D15	FPGPIO
B14	FPD34	**D16**	**VDDCORE**
B15	FPDE/MOD	D17	PD33
B16	PD61	D18	PD34
B17	PD58	D19	PD55
B18	PD47	D20	PD48
B19	PD44	E1	AR
B20	PD41	E2	AVSS
C1	VREF	E3	COMP
C2	**CLKAVSS1**	**E4**	**CLKAVSS2**

Table 3-3. Numerical Pin Listing (Continued)

Number	Name	Number	Name
E17	PD32	K3	LD5
E18	PD35	**K4**	**VSSCORE**
E19	PD54	**K9**	**VSSPAD1**
E20	PD49	**K10**	**VSSPAD2**
F1	**AVDD**	**K11**	**VSSPAD2**
F2	AG	**K12**	**VSSPAD2**
F3	AB	K17	$\overline{RAS0}$/$\overline{CS1}$/MA10
F4	AY	K18	$\overline{CAS7}$/DQM7
F17	**VDDMEM5**	K19	$\overline{OE}$/$\overline{SDCAS}$
F18	PD36	K20	SDCLK
F19	PD53	L1	$\overline{CREQ}$/CRDY/VS
F20	PD50	L2	LD6
G1	**TVDACVDD**	L3	LD7
G2	AC	**L4**	**VDDCORE**
G3	**TVDACVSS**	**L9**	**VSSPAD1**
G4	**CLKAVSS3**	**L10**	**VSSPAD1**
G17	**VDDMEM**	**L11**	**VSSPAD2**
G18	PD37	**L12**	**VSSPAD2**
G19	PD52	L17	$\overline{RAS1}$/$\overline{SDRAS}$
G20	PD51	L18	MA8
H1	HSYNC	L19	MA7
H2	VSYNC	L20	MA0
H3	LD0	M1	LCLK/VCLK
H4	**VDDLPB5**	M2	SPCLK
H17	$\overline{CS0}$	M3	SPDAT
H18	PD38	M4	PWM1/$\overline{ODD}$
H19	PD39	**M9**	**VSSPAD1**
H20	$\overline{CAS4}$/DQM4	**M10**	**VSSPAD1**
J1	LD1	**M11**	**VSSPAD1**
J2	LD2	**M12**	**VSSPAD1**
J3	LD3	M17	MA9
J4	**VDDLPB**	M18	MA2
J9	**VSSPAD2**	M19	MA6
J10	**VSSPAD2**	M20	MA1
J11	**VSSPAD2**	N1	LPBEN/EMCLK
J12	**VSSPAD2**	N2	LD8
J17	$\overline{WE}$	N3	LD9
J18	$\overline{CAS6}$/DQM6	N4	EDCLK2
J19	$\overline{CAS5}$/DQM5	**N17**	**VDDMEM**
J20	SDCLKI	N18	MA5
K1	$\overline{VREQ}$/VRDY/HREF	N19	MA4
K2	LD4	N20	MA3

Table 3-3. Numerical Pin Listing (Continued)

Number	Name	Number	Name
P1	LD10	U19	PD24
P2	LD11	U20	PD11/RA11
P3	LD12	V1	AD31
P4	LD13	V2	AD29
P17	**VSSCORE**	V3	C/BE3
P18	PD26	V4	AD21
P19	PD13/RA13	V5	AD18
P20	PD8/RA8	V6	AD16
R1	LD14	V7	IRDY
R2	LD15	V8	PAR
R3	RESET	V9	AD12
R4	REQ	V10	AD9
R17	DSF	V11	AD7
R18	PD27	V12	AD4
R19	PD14/RA14	V13	AD1
R20	PD9/RA9	V14	CAS1/DQM1
T1	CLK32	V15	PD7/RA7
T2	STANDBY	V16	PD2/RA2
T3	SUSPEND	V17	PD1/RA1
T4	**VDDSYS**	V18	PD30
T17	PD31	V19	PD25
T18	PD28	V20	PD12/RA12
T19	PD15/RA15	W1	AD30
T20	PD10/RA10	W2	AD28
U1	SCLK	W3	AD24
U2	INTA	W4	AD22
U3	AD25	W5	AD19
U4	AD23	W6	FRAME
U5	GNT	W7	DEVSEL
U6	**VDDSYS**	W8	AD15
U7	**VDDSYS5**	W9	AD13
U8	STOP	W10	AD10
U9	AD14	W11	C/BE0
U10	**VSSCORE**	W12	AD5
U11	NO CONNECT	W13	AD2
U12	NO CONNECT	W14	CAS2/DQM2
U13	CLKRUN	W15	PD6/RA6
U14	CAS0/DQM0	W16	PD3/RA3
U15	SDCLKEN	W17	PD23/RD7
U16	**VDDCORE**	W18	PD22/RD6
U17	PD0/RA0	W19	PD21/RD5
U18	PD29	W20	PD20/RD4

Table 3-3. Numerical Pin Listing (Continued)

Number	Name
Y1	AD27
Y2	AD26
Y3	IDSEL
Y4	AD20
Y5	AD17
Y6	$\overline{C/BE2}$
Y7	$\overline{TRDY}$
Y8	$\overline{C/BE1}$
Y9	AD11
Y10	AD8
Y11	AD6
Y12	AD3
Y13	AD0
Y14	$\overline{CAS3}$/DQM3
Y15	PD5/RA5
Y16	PD4/RA4
Y17	PD19/RD3
Y18	PD18/RD2
Y19	PD17/RD1
Y20	PD16/RD0

Section 4: Electrical Data

4.1 MAXIMUM RATINGS

Table 4-1. Absolute Maximum Ratings

Ambient temperature	0° C to 70° C
Storage temperature	-40° C to 125° C
DC Supply Voltage	-0.5V to 5.0V
I/O Pin Voltage with respect to V_{SS}	-0.5V to V_{DD}+0.5V

4.2 DC SPECIFICATIONS

Note: With mixed voltage operation, the 5V power plane must always be at a higher voltage than the 3.3V power plane.

Note: In all cases below, digital VDD = 3.3V ± 5% and the operating temperature is 0° C to 70° C.

Table 4-2. RAMDAC/TVDAC/Clock Synthesizer DC Specifications

Symbol	Parameter	Min	Typical	Max	Unit
AVDD	DAC supply voltage	3.135	3.3	3.465	V
AVDD (CLOCK)	PLL supply voltage	3.135	3.3	3.465	V
VREF	Internal voltage reference	1.10	1.23	1.35	V
IAVDD	DAC Supply Current		60		mA
IAVDD (CLOCK)	PLL Supply Current		15		mA

Table 4-3. RAMDAC Characteristics

	Min	Typical	Max	Unit
Resolution Each DAC		8		bits
LSB Size		66		µA
Integral Linearity Error			± 1	LSB
Differential Linearity Error			± 1	LSB
Output Full-Scale Current (no pedestal)	15.4	17.6	19.8	mA
Output Full-Scale Current (pedestal)	16.85	19.05	21.25	mA
DAC to DAC Mismatch			5%	
Power Supply Rejection Ratio			0.5	%/ % AVDD
Output Compliance	0.0		1.5	V
Output Capacitance			30	pF
Glitch Impulse		75		pV-Sec

Table 4-4. RAMDAC Output Specifications

Description	I_{OUT} (mA)	V_{OUT} (V)	BLANK	Input Data
White (with $\overline{BLANK}$ pedestal)	19.05 (typical)	0.714 (typical)	1	FFH
White	17.6 (typical)	0.66 (typical	1	FFH
Data (with pedestal)	Data + 1.45	Data + 0.054	1	Data
Data	Data	Data	1	Data
Black (with pedestal)	1.45 (typical)	0.054	1	00H
Black (no pedestal)	0	0	1	00H
$\overline{BLANK}$	0	0	0	Don't Care

Notes

1. Condition for V_{OUT} is a 75 Ohm doubly terminated load, use of the internal VREF and RSET = 147 Ohms.
2, No sync pedestal is provided. Sync output levels are the same as for black output.
3. The $\overline{BLANK}$ pedestal is active when SR27_3 = 1.

Table 4-5. TVDAC Characteristics

	Min	Typical	Max	Unit
Resolution Each DAC		9		bits
LSB Size		69.1		µA
Integral Linearity Error			± 1	LSB
Differential Linearity Error			± 1	LSB
Output Full-Scale Current	31.6	35.1	38.6	mA
DAC to DAC Mismatch			5%	
Power Supply Rejection Ratio			0.5	%/ % AVDD
Output Compliance	0.0		1.5	V
Output Capacitance			30	pF
Glitch Impulse		75		pV-Sec

Note

1. Condition for LSB and output full scale current is a 75 Ohm doubly terminated load, use of the internal VREF, RSET = 147 Ohms and SR1A_7 = 1.

Table 4-6. Digital DC Specifications

VDD = 3.3V ± 5% for all pins except 5V tolerance pins if they are enabled for 5V tolerance, 5V ± 5% for the three 5V tolerance pins if they are enabled for 5V tolerance. Operating Temperature 0° C to 70° C

Symbol	Parameter	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage	-0.5		0.99	V
V_{IH}	Input High Voltage	1.65		5.5 (Note 1)	V
V_{OL}	Output Low Voltage			0.5	V
V_{OH}	Output High Voltage	2.1			V
I_{OL}	Output Low Current	Note 2			mA
I_{OH}	Output High Current	Note 3			mA
I_{OZ}	Output Tri-state Current			1	µA
C_{IN}	Input Capacitance			5	pF
C_{OUT}	Output Capacitance			5	pF
I_{CC}	Power Supply Current		275 (Note 4)		mA

Notes

1. If 5V tolerance is enabled. Otherwise, this is 3.6V.
2. Drive strengths are given for each output in Table 3-1.
3. This value is -1/2 the drive level listed for each output in Table 3-1.
4. Typical I_{CC} measured for an XGA panel displaying a DOS prompt.

4.3 AC SPECIFICATIONS

4.3.1 RAMDAC AC Specifications

Table 4-7. RAMDAC AC Specifications

Load: 75Ω doubly terminated with 80 pF

Parameter	Typical	Max	Unit	Notes
DAC Output Delay	5		ns	1
DAC Output Rise/Fall Time	3		ns	2
DAC Output Settling Time	15		ns	
DAC-to-DAC Output Skew	2	5	ns	3

Notes

1. Measured from the 50% point of VCLK to the 50% point of full scale transition
2. Measured from 10% to 90% full scale
3 With DAC outputs equally loaded

Table 4-8. TVDAC AC Specifications

Load: 75Ω doubly terminated with 80 pF

Parameter	Typical	Max	Unit	Notes
DAC Output Delay	5		ns	1
DAC Output Rise/Fall Time	3		ns	2
DAC Output Settling Time	15		ns	
DAC-to-DAC Output Skew	2	5	ns	3

Notes

1. Measured from the 50% point of TVCLK to the 50% point of full scale transition
2. Measured from 10% to 90% full scale
3 With DAC outputs equally loaded

4.3.2 Clock Timing

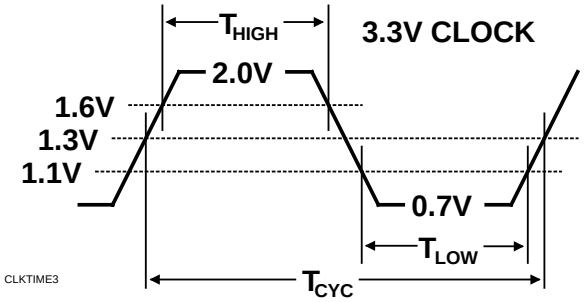


Figure 4-1. Clock Waveform Timing

Table 4-9. Clock Waveform Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{CYC}	SCLK Cycle Time	15	125	ns	1
	LCLK Cycle Time	25	200	ns	
	MCLK Cycle Time (1-cycle EDO)	16.67	25	ns	
	DCLK Cycle Time (CRT VGA Mode)	25	50	ns	
	DCLK Cycle Time (CRT Enhanced Mode)	7.4	50	ns	
	DCLK Cycle Time (TFT Panel)	9.1	50	ns	
	DCLK Cycle Time (STN Panel)	12.5	50	ns	
	SDCLK Cycle Time	12	25	ns	
T_{HIGH}	SCLK High Time	6	80	ns	
	LCLK High Time	12	160	ns	
	SDCLK High Time	3.5	80	ns	
T_{LOW}	SCLK Low Time	6	80	ns	
	LCLK Low Time	12	160	ns	
	SDCLK Low Time	3.5	80	ns	
	SCLK, LCLK, SDCLK Slew Rate	1	4	V/ns	2

Notes

1. If there is no internal activity using SCLK, it can be shut off to reduce power consumption.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to peak portion of the clock waveform.

4.3.3 Input/Output Timing

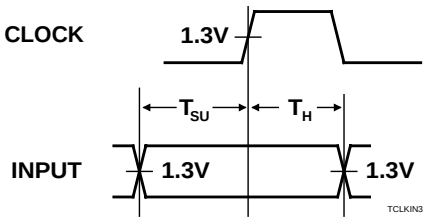


Figure 4-2. Input Timing

Table 4-10. SCLK-Referenced Input Timing

PCI Bus			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	All inputs setup	7	ns
T_H	All inputs hold	0	ns
AGP Bus (1X)			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	All inputs setup	5	ns
T_H	All inputs hold	0	ns
Miscellaneous			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	ROM data RD[7:0] setup	5	ns
T_H	ROM data RD[7:0] hold	7	ns

Table 4-9. LCLK-Referenced Input Timing

Bidirectional Interface			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	LD[7:0] setup	10	ns
T_H	LD[7:0] hold	9	ns
T_{SU}	$\overline{CREQ}$/CRDY	6	ns
T_H	$\overline{CREQ}$/CRDY	8	ns
Digitizer Interface (Video 8/16)			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	LD[15:0] setup	6	ns
T_H	LD[15:0] hold	8	ns
T_{SU}	HS setup	6	ns
T_H	HS hold	7	ns
T_{SU}	VS setup	6	ns
T_H	VS hold	7	ns
T_{SU}	$\overline{ODD}$ setup	6	ns
T_H	$\overline{ODD}$ hold	8	ns

Table 4-10. MCLK-Referenced Input Timing

Symbol	**Parameter**	**Min**	**Units**
T_{SU}	PD[63:0] setup to following $\overline{CAS}$ low (1-cycle EDO)	0	ns
T_H	PD[63:0] hold from following $\overline{CAS}$ low (1-cycle EDO)	15	ns

Note

1. The $\overline{CAS}$ signals used to latch read data are derived from the internal MCLK.

Table 4-11. SDCLK-Referenced Input Timing

Note: SDCLKI is the reference for MCLK > 66 MHz

Symbol	**Parameter**	**Min**	**Units**
T_{SU}	PD[63:0] setup	1	ns
T_H	PD[63:0] hold	2.5	ns

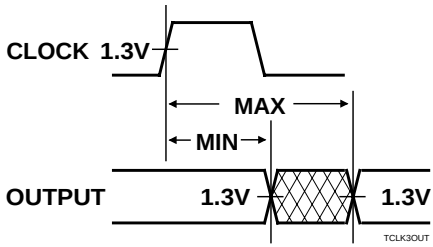


Figure 4-3. Output Timing

The minimum delay is the minimum time after the clock edge that the valid signal state from the previous cycle will begin transition to the next state (become invalid).

The maximum delay is the maximum time after the clock edge that the signal state is valid for the next cycle.

Table 4-12. SCLK-Referenced Output Timing

PCI Bus					
Parameter	**Min**	**Max**	**Units**	**Load (pF)**	**Notes**
AD[31:0] valid delay	2	16	ns	50	1
Other PCI signals delay	2	11	ns	50	1, 2
AGP Bus (1X)					
Parameter	**Min**	**Max**	**Units**	**Load (pF)**	**Notes**
All signals delay	1.5	6	ns	10	3
Float to active delay	1.5	6	ns	10	3
Active to float delay	1	14	ns	10	3
Miscellaneous					
Parameter	**Min**	**Max**	**Units**	**Load (pF)**	**Notes**
$\overline{\text{ROMEN}}$ delay	4	10	ns	50	
ROM address valid delay	5	30	ns	30	
AD[7:0] ROM data valid delay	5	30	ns	50	

Notes

1. Maximum delays for PCI signals are based on the 33 MHz PCI specification.
2. Medium $\overline{\text{DEVSEL}}$ timing used
3. Maximum delays for AGP bus operation are based on the AGP 1.0 specification.

Table 4-13. LCLK-Referenced Output Timing

Scenic/MX2 Interface					
Parameter	**Min**	**Max**	**Units**	**Load (pF)**	**Notes**
$\overline{\text{VREQ}}$/VRDY active delay	2	11	ns	20	7 ns typ
LD[7:0] valid delay	2	15	ns	20	8 ns typ
LD[7:0] tri-state from LCLK	7	15	ns	20	

Table 4-14. MCLK-Referenced Output Timing (EDO)

Parameter	**Min**	**Max**	**Units**	**Load (pF)**	**Notes**
PD[63:0] valid delay	2	7	ns	20	
MA[8:0] valid delay	1.5	8	ns	45	
$\overline{\text{CAS[7:0]}}$ active delay	1	5.5	ns	25	
$\overline{\text{CAS[7:0]}}$ inactive delay	1	5.5	ns	25	
$\overline{\text{RAS[1:0]}}$ active delay	1	5	ns	40	
$\overline{\text{RAS[1:0]}}$ inactive delay	1	6.5	ns	40	
$\overline{\text{OE[1:0]}}$ active delay	1.5	4.5	ns	40	
$\overline{\text{WE}}$ active delay	1.5	4.5	ns	40	

Table 4-15. SDCLK-Referenced Output Timing (SGRAM)

Parameter	**Min**	**Max**	**Units**	**Load (pF)**	**Notes**
PD[63:0] valid delay	4	6	ns	20	
MA[10:0] valid delay	4	6	ns	40	
DQM[7:0], $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{CS[1:0]}}$, $\overline{\text{WE}}$ active delay	4	6	ns	40	

Table 4-16. FPSCLK-Referenced Output Timing

Parameter	Min	Max	Load(pF)	Units	Notes
FPD[36:0], FPDE, FPPOL delay	0	3	25	ns	1, 2
FPD[36:0], FPDE, FPPOL delay	0	10	80	ns	1
FPVSYNC, FPHSYNC active delay	0	10	80	ns	

Notes:

1. This delay assumes that SR40_3-1 is programmed to 000b (no FPSCLK delay), SR3D_6 and SR3D_7 are programmed to 1 and the output loading on FPSCLK is approximately the same as the FPD load.
2. This is applicable if driving an external data transmitter.

4.3.4 Reset Timing

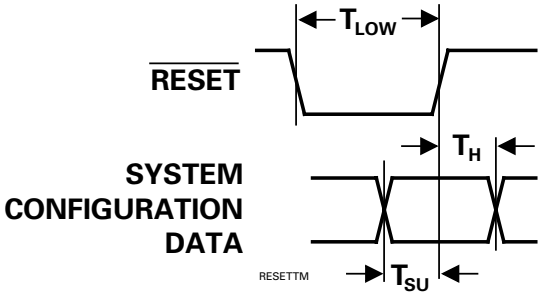


Figure 4-4. Reset Timing

Table 4-17. Reset Timing

Symbol	Parameter	Min	Units
T_{LOW}	$\overline{RESET}$ active pulse width	1000	ns
T_{SU}	PD[31:0] setup to $\overline{RESET}$ inactive	20	ns
T_H	PD[31:0] hold from $\overline{RESET}$ inactive	10	ns

Section 5: Reset and Power Control

The $\overline{\text{RESET}}$ signal resets the internal state machines and places all registers in their power-on default states.

5.1 CONFIGURATION STRAPPING

The PD[31:0] pins are pulled low internally and can be individually pulled high through 10 KΩ resistors. These pull-ups and pull-downs do not affect normal operation of the pins as part of the pixel data bus, but they do force the pins to a definite state during reset. At the rising edge of the reset signal, this state is sampled, the result is inverted and the data loaded into the CR36, CR37, CR68 and CR6F registers. The data is used for system configuration. The definitions of the PD[31:0] strapping bits at the rising edge of the reset signal are shown in Table 5-1.

Important Note: As described above, the signal levels on PD[31:0] are inverted before being latched in the various strapping bit registers. Since PD[31:0] all have internal pull-downs, the default values for each of the strapping bits is 1. The value latched at reset can be changed to 0 by adding an external pull-up to the appropriate pin. After reset, the strapping bits are written and read normally, i.e., there is no inversion of the register values.

Strapping bits 7-6 define the display memory size. However, the BIOS determines this value directly and writes it to CR36_7-6 after reset. Therefore, systems do not need to strap the PD[7:6] pins. Other pins may also not require strapping, depending on the design.

Table 5-1. Definition of Strapping Bits at the Rising Edge of the Reset Signal

Note: The CR Bit Values in this table are the latched values as software would read or write them. To latch a 0 at reset, an external pull-up resistor must be connected to the appropriate PD pin as explained by the note on the previous page.

CR Bits	PD Pins	CR Bit Value	Function
CR36_0	**$\overline{\text{INTA}}$ Claim**		
	0	0	PCI register at offset 3DH reads 01H (INTA used as interrupt pin)
		1	PCI register at offset 3DH reads 00H (no interrupt claimed)
CR36_3-2	**Memory Type**		
		00	Reserved
		01	1-cycle EDO
		10	Reserved
		11	SDRAM/SGRAM
	Display Memory Size		
CR36_7-5	7-5	000	4 MBytes (1Mx16 SDRAM). 64-bit interface. This is the only setting that requires strapping. If the BIOS reads 000b (PD[7-5] all pulled up), it does not overwrite this value.
		001	4 MBytes (1Mx16 SDRAM). 32-bit interface. (no strapping required)
		010	4 MBytes (SGRAM or EDO). (no strapping required)
		110	2 MBytes (SGRAM or EDO). (no strapping required
			All other values reserved.
CR37_0	**Disable I/O Access**		
	8	0	Disable I/O access. 3C3H_0 is forced to 1 and PCI04_0 is ignored.
		1	Normal I/O access can be enabled (PCI04_0 = 1)
	NAND-tree Scan		
CR37_1	9	0	Allows testing for bad solder connections
		1	Normal operation
	Subsystem ID Source		
CR37_2	10	0	Read subsystem ID information from CR95-CR98
		1	Read subsystem ID information from the ROM BIOS
CR37_4	**ACPI D1 State**		
	12	0	ACPI D1 state allowd
		1	ACPI D1 state not allowed
CR37_5	**IDSEL Connection**		
	13	0	IDSEL connected internally to AD16 (add-in card)
		1	IDSEL connected internally to AD17 (motherboard)
CR37_6	**AGP Operation**		

Table 5-1. Definition of Strapping Bits at the Rising Edge of the Reset Signal (Continued)

CR Bits	PD Pins	CR Bit Value	Function
	14	0	AGP enabled (this must be strapped for all designs)
		1	Not allowed
CR37_7	**ACPI D2 State**		
	15	0	ACPI D2 state allowd
		1	ACPI D2 state not allowed
		1	7 MCLKs
	Memory Type Select (SDRAM/SGRAM)		
CR68_7-6	23-22	00	Reserved
		01	256Kx32 SGRAM
		10	512Kx32 SGRAM
		11	1Mx16 SDRAM
	SDRAM/SGRAM Clock Select		
CR6F_7	31	0	Internal clock used to latch read data
		1	SDCLKR used to latch read data

Table 5-1. Definition of Strapping Bits at the Rising Edge of the Reset Signal (Continued)

5.2 NAND-TREE SCAN

NAND-tree scanning is enabled when PD9 is pulled high at reset. All digital pins become inputs except the SPCLK pin (M2) and the $\overline{\text{RESET}}$ pin (R3). SPCLK is the output pin for the boundary scan and $\overline{\text{RESET}}$ cannot be tested and must not be connected.

The tester drives high logic to all digital inputs. It then sequentially drives and holds each input low and records the state of the SPCLK pin. If all pin connections are good, the output will be a perfect square wave. If this pattern is broken, the location of the incorrect signal level in the sequence identifies the bad connection.

The digital inputs to be tested are all pins except the following:

SPCLK
$\overline{\text{RESET}}$
XIN
XOUT
VREF
COMP
RSET
AR
AB
AG
AY
AC
All analog and digital powers and grounds

The connections must be tested in the signal order given in Table 5-2. The first column is tested first, the second column next, etc.

Table 5-2. NAND-tree Scan Order

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
M3	SPDAT	Y11	AD6	M17	MA9	D14	FPD32
M4	PWM1	W11	C/BE0	L20	MA0	A13	FPD31
N1	LPBEN	V11	AD7	L19	MA7	B13	FPD30
N2	LD8	Y12	AD3	L18	MA8	C13	FPD29
N3	LD9	W12	AD5	L17	RAS1	A12	FPD28
N4	EDCLK2	V12	AD4	K17	RAS0	B12	FPD27
P1	LD10	Y13	AD0	K19	OE	C12	FPD26
P2	LD11	W13	AD2	J19	CAS5	D12	FPD25
P3	LD12	V13	AD1	K20	SDCLK	A11	FPD24
P4	LD13	K18	CAS7	J17	WE	B11	FPD23
R1	LD14	J18	CAS6	V14	CAS1	C11	FPD22
R2	LD15	Y14	CAS3	H20	CAS4	A10	FPD21
R4	REQ	W14	CAS2	J20	SDCLKI	B10	FPD20
T1	CLK32	U19	PD24	U14	CAS0	C10	FPD19
T2	STANDBY	D19	PD55	H19	PD39	D10	PWM0
T3	SUSPEND	A18	PD56	C20	PD40	A9	FPD18
U2	INTA	U15	SDCLKEN	H17	CS0	B9	FPD17
U1	SCLK	W17	PD23	V15	PD7	C9	FPD16
V1	AD31	C16	PD62	P20	PD8	A8	FPD15
W1	AD30	A15	PD63	B20	PD41	B8	FPD14
V2	AD29	A17	PD57	W15	PD6	C8	FPD13
U3	AD25	B17	PD58	R20	PD9	D8	FPD12
Y1	AD27	E19	PD54	H18	PD38	A7	FPD11
W2	AD28	V19	PD25	Y15	PD5	B7	FPD10
V3	C/BE3	F19	PD53	T20	PD10	C7	FPD9
U4	AD23	C17	PD59	G18	PD37	A6	FPD8
Y2	AD26	W18	PD22	A20	PD42	B6	FPD7
W3	AD24	P18	PD26	Y16	PD4	C6	FPD6
V4	AD21	G19	PD52	U20	PD11	D6	FPD5
U5	GNT	A16	PD60	W16	PD3	A5	FPD4
Y3	IDSEL	W19	PD21	V16	PD2	B5	FPD3
W4	AD22	R18	PD27	V20	PD12	C5	FPD2
V5	AD18	G20	PD51	F18	PD36	A4	FPD1
Y4	AD20	W20	PD20	V17	PD1	B4	FPD0
W5	AD19	T18	PD28	P19	PD13	A3	FPVSYNC
Y5	AD17	Y17	PD19	E18	PD35	C4	FPHSYNC
V7	IRDY	Y18	PD18	A19	PD43	B3	FPSCLK
Y6	C/BE2	U18	PD29	R19	PD14	A2	ENAVDD
W6	FRAME	F20	PD50	D18	PD34	D4	STWR
V6	AD16	B16	PD61	B19	PD44	C3	ENAVEE
U8	STOP	Y19	PD17	D17	PD33	H1	HSYNC
Y7	TRDY	V18	PD30	C19	PD45	H2	VSYNC
W7	DEVSEL	E20	PD49	B18	PD47	H3	LD0
U9	AD14	R17	DSF	C18	PD46	J1	LD1
Y8	C/BE1	Y20	PD16	E17	PD32	J2	LD2
W8	AD15	T17	PD31	T19	PD15	J3	LD3
V8	PAR	D20	PD48	U17	PD0	K1	VREQ/VRDY
Y9	AD11	N20	MA3	B15	FPDE	K2	LD4
W9	AD13	N19	MA4	C15	FPPOL	K3	LD5
V9	AD12	N18	MA5	D15	FPGPIO	L1	CREQ/CRDY
Y10	AD8	M20	MA1	A14	FPD35	L2	LD6
W10	AD10	M19	MA6	B14	FPD34	L3	LD7
V10	AD9	M18	MA2	C14	FPD33	M1	LCLK

5.3 FLAT PANEL POWER SEQUENCING

The flat panel may be damaged if the bias voltage VEE is applied to the liquid crystal material without enabling the control and data signals to the panel, which require VDD. ViRGE/MX supplies the ENAVDD and ENAVEE signals to control power up/down sequencing of LCD panels. These signals drive external power management components which eventually drive panel VDD and panel VEE.

At the end of a power down sequence, ViRGE/MX is in its idle power down state. This status is indicated by SR46_6. After power up or a system reset, ViRGE/MX stays in idle power down state. The BIOS must program SR31_4 = 1 to enable flat panel operation. This initiates a power up sequence. Disabling flat panel display (clearing SR31_4 to 0) automatically generates a panel power down sequence. Similarly, entering Standby or Suspend initiates a power down sequence and leaving Standby or Suspend initiates a power up sequence.

Sequencing timing is shown in Figure 5-1. The t_1 and t_2 values can each be programmed to 32 or 128 ms via bits 2 and 3 of SR41. The default is 32 ms for both t_1 and t_2.

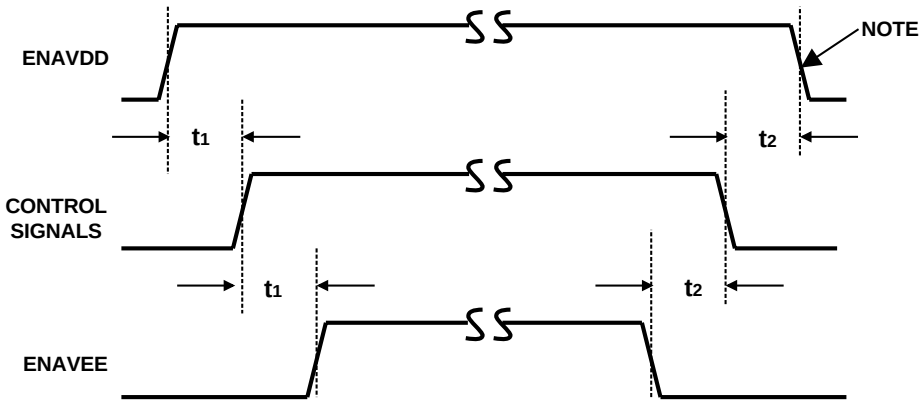
At the end of a power up sequence, ViRGE/MX is in its idle power up state. This status is indicated by SR46_7.

The PWM{1:0] signals, which can control panel contrast and brightness, are also sequenced. See Figure 11-8.

5.4 POWER MANAGEMENT

The operational modes can be classified by the following three categories:

- Normal mode
- Standby mode
- Suspend mode



NOTE: CLK32 MUST BE VALID FOR AT LEAST 4 CLOCK CYCLES AFTER ENAVDD IS DEASSERTED WHEN ENTERING STANDBY AND AT LEAST 6 CLOCK CYCLES WHEN ENTERING SUSPEND. PWRSEQ

Figure 5-1. Flat Panel Power Sequencing

5.4.1 Normal Mode

During the Normal mode of operation, the flat panel is active. The CPU can access video memory and I/O registers and normal refresh to the video memory is provided. In this mode, ViRGE/MX provides a number of automatic power management functions. These turn off power to certain internal blocks when these blocks are inactive.

5.4.2 Standby Mode

In Standby, ViRGE/MX suspends all display-related memory activities. The CPU can still access video memory and I/O registers. In summary, the following occur in Standby mode:

- Dot clocks on various blocks can be gated off
- CRT and/or TV DAC can be powered down
- The CPU can access and modify the video display memory and CLUTs

Standby mode is controlled by three different methods. These are:

- STANDBY input pin, a bit defining the operation of this pin and a hardware Standby enable bit
- Activity bit
- Software Standby bit

The function of the STANDBY pin is enabled when SR42 _4 is set to 1. The activity function is enabled by setting SR43_6 to 1. This means that internal chip activity (register access, Graphic Engine busy, etc.) is used as a criterion for entering or leaving Standby. Software Standby is controlled by SR42_5. Only one of these functions should be enabled/used at a time. The activity function provides additional flexibility and may not be required.

The second Standby setup function is to specify a timeout value controlling the time between initiation of Standby and the actual entering of that state. The Standby timer is programmed with a timeout value in SR43_5-0, with SR41_7-6 specifying the timeout value.

The STANDBY pin has two operational modes. If SR44_4 = 0 and hardware Standby is enabled, the Standby sequence is initiated by a low to high transition on the STANDBY pin. This starts the timeout counter. If the STANDBY pin remains in a high logic state until the timer expires and a panel power down sequence is completed (see Section 5.3), the system enters Standby. If the STANDBY pin transitions from high to low before the idle power down state is reached, a power up sequence is generated (if required), the timer is reset and normal operation continues.

Once in Standby state, a high to low transition of the STANDBY pin initiates exiting of this state. This transition causes a panel power on sequence. When this is complete, normal operation is restored and the timer is reset.

If SR44_4 = 1, the Standby timeout counter begins counting when hardware Standby is enabled (SR42_4 = 1). If the STANDBY pin is not taken from low to high before the timer expires and the power down sequence is complete, the system enters Standby. Every rising edge of the Standby pin will either reset the timer (if not in Standby) or take the system out of Standby. Thus, in this mode, the STANDBY pin becomes an activity pin. As soon as Standby is exited and the power up sequence is complete, the Standby timer resets and starts counting again. The activity pulses on the STANDBY pin must be exactly 4 SCLKs wide.

Summarizing, if SR44_4 = 0, driving the STANDBY pin high initiates Standby mode and driving it low initiates exiting of Standby. If SR44_4 = 1, the system is always trying to go into Standby mode and 4 SCLK high pulses on the STANDBY pin either prevent this or take the system out of Standby, resetting the timer in either case.

If the activity function is enabled, this starts the timeout counter. If no internal chip activity is detected before the timer expires, a panel power down sequence is initiated. At the end of the power down sequence, the Standby state is entered. If activity is detected before the timer expires, the timer is reset and counting restarts. This sequence continues as long as the activity function is enabled. Once in Standby state, any chip activity causes a panel power on sequence. When this is complete, normal operation is restored except that the Standby timeout counter is again active.

If the software Standby bit (SR42_5) is set, this starts the timeout counter. If the bit is not cleared before the timer expires, the Standby state entry sequence is executed. If the software Standby bit is cleared before the timer expires, the timer is reset and normal operation continues. Once in Standby state, clearing the software Standby bit to 0 causes a panel power on sequence. When this is complete, normal operation is restored.

If Standby is initiated while any chip activity is in progress, any current transaction is completed first.

If a power up sequence is requested while a power down sequence is being executed, it will be delayed and executed immediately after the power down sequence completes. Power up sequences do not use the timer. If the system is already in its idle power down state (SR46_6 reads 1) when a Suspend request is made, the power down sequence will not be done.

Standby mode status can be read via SR46 _5
(0 = off; 1 = on).

5.4.3 Suspend Mode

The following occur in Suspend mode:

- Register data bits are retained
- DCLK and MCLK oscillators are shut off
- Only PCI configuration cycle accesses are allowed (SR1E_7 must be set to 1 to disable all CPU accesses)
- EDO DRAM put in self or slow refresh mode
- SDRAM/SGRAM put in self refresh mode or power down mode
- All pins are deactivated except for the SUSPEND and DRAM control pins
- CRT and TV DAC are powered down

Suspend mode is controlled by two different methods. These are:

- SUSPEND input pin
- Software Suspend bit

When hardware Suspend is used, the Suspend debounce timer is programmed with a value of 62.5 µs (SR42_7-6 = 00b) or 2 seconds (SR42_7-6 = 01b). The Suspend sequence is initiated by a low to high transition of the SUSPEND pin. If after the debounce period, the SUSPEND pin is still high, a power

down sequence is initiated (if the system is not already in its idle power down state) followed by entry to the Suspend state.

Software-initiated Suspend is entered by setting SR42_1 to 1. Since CPU access is not allowed in Suspend mode, exiting requires that the SUSPEND pin be driven from high to low. Exiting of Suspend clears SR42_1 to 0. The CLK32 signal must be valid when the SUSPEND pin is deasserted or toggled.

If supported by the DRAMs, slow EDO DRAM refresh can be selected (CR74_3-1 = 1xxb). This uses the 32 KHz clock. If supported, the DRAM will be placed in self refresh mode (CR74_3-1 = 000b). Burst refresh before and after self refresh can be enabled via CR74_4 and CR74_5. SDRAM/SGRAM can be put in power down mode (CR74_3-1 = 001b). The 32 KHz clock can be stopped after the power down sequencing for all modes except slow EDO DRAM refresh. It must be reenabled before power up sequencing. The system BIOS must program the correct choice of refresh type supported by the DRAM.

If Suspend mode is initiated while any chip activity is in progress, any current transaction is completed first. If Suspend mode is initiated while the chip is in Standby mode, Standby is interrupted and resumed (assuming the request is still active) after leaving Suspend.

Several register bits control the states of HSYNC and VSYNC during Susepend (and Standby). Table 5-3 shows these states when display power management (DPMS) is being used.

Table 5-3 Suspend Sync States When Using Display Power Management (DPMS)

	SRD_5-4 = 01	SRD_5-4 = 10	SRD_7-6 = 01	SRD_7-6 = 10
HSYNC State	LOW	HIGH	N/A	N/A
VSYNC State	N/A	N/A	LOW	HIGH

If DPMS is not being used (SRD_5-4 = 00 for HSYNC, SRD_7-6 = 00 for VSYNC), the states are shown in Tables 5-4 and 5-5

Table 5-4 Suspend HSYNC States When DPMS is Not Used

HSYNC State	3C2_6 (CRT only or DuoView) SR32_1 (LCD/CRT Simultaneous	SR42_0
LOW	0	1
HIGH	1	1
32 kHz	Don't Care	0

Table 5-5 Suspend VSYNC States When DPMS is Not Used

VSYNC State	3C2_7 (CRT only or DuoView) SR32_2 (LCD/CRT Simultaneous	SR42_0
LOW	0	1
HIGH	1	1
32 kHz	Don't Care	0

The appropriate bits must be set by the BIOS before hardware Suspend is entered.

5.4.4 Hibernate Mode

Hibernate mode is executed by the system. It is entered when the system reads the contents of the registers and DRAM and stores it to disk before activating Suspend. Once the data is saved, power to ViRGE/MX can be turned off. The stored data is used after power-on reset to return ViRGE/MX to its operating state before entering Hibernate mode. Note that the S3d and many of the Streams Processor registers are shadowed, which means they cannot be accurately read. The system must keep track of writes to these registers in order to be able to restore them properly.

5.4.5 Pin States During Suspend and Reset

Outputs can have four states:

Tri-state
Driven high
Driven low
Driven at level upon entering Suspend

Inputs have two states:

Disabled - The pin can be left floating without consuming power
Enable - The pin must be driven externally (will consume power if left floating)

Table 5-3. Pin States During Suspend and Reset

Pin(s)	Suspend State	Reset State
AB	Analog	Analog
AC	Analog	Analog
AD[31:16]	Tristate/Disable	Tristate/Enable
AD[15:0]	Tristate/Disable	Tristate/Enable
AG	Analog	Analog
AR	Analog	Analog
AY	Analog	Analog
CAS[7:0]	Note 2/Disable	High/Disable
C/BE[3:0]	Tristate/Disable	Tristate/Enable
CLK32	Input - Enable	Input - Enable
COMP	Analog	Analog
CREQ/CRDY	Tristate/Disable	Tristate/Enable
CS[1:0]	Note 2/Disable	High/Disable
CSYNC	Note 6/Disable	Tristate/Disable
DBF	Tristate/Disable	Tristate/Enable
DEVSEL	Tristate/Disable	Tristate/Enable
DQM[7:0]	Note 2/Disable	High/Disable
DSF	Low/Disable	Low/Disable
EDCLK[1:2]	Low/Disable	Tristate/Enable
EMCLK	Low/Enable	Tristate/Enable
ENAVDD	Low/Disable	Low/Disable
ENAVEE	Low/Disable	Low/Disable
FLM	Low/Disable	Low/Disable
FPD[35:27]	Low/Disable	Low/Disable
FPD[26:18]	Low/Disable	Low/Disable
FPD[17:9]	Low/Disable	Low/Disable
FPD[8:0]	Low/Disable	Low/Disable

FPDE	Low/Disable	Low/Disable
FPGPIO	Note 4/Disable	Tristate/Enable
FPHSYNC	Low/Disable	Low/Disable
FPPOL	Low/Disable	Low/Disable (Note 9)
FPSCLK	Low/Disable	Low/Disable
FPVSYNC	Low/Disable	Low/Disable
$\overline{\text{FRAME}}$	Tristate/Disable	Tristate/Enable
$\overline{\text{GNT}}$	Input - Disable	Input - Enable
GOP0	Driven/Disable	Driven/Disable
HS	High/Disable	Tristate/Enable
HSYNC	Note 6/Disable	Tristate/Disable
IDSEL	Input - Disable	Input - Enable
$\overline{\text{INTA}}$	Tristate/Disable	Tristate/Disable
$\overline{\text{IRDY}}$	Tristate/Disable	Tristate/Enable
LCLK	Driven/Disable	Tristate/Enable
LD[15:7]	Input - Disable	Input - Disable
LD[7:0]	Tristate/Disable	Tristate/Enable
LP	Low/Disable	Low/Disable
LPBEN	Low/Enable	Tristate/Enable
MA[10:0]	Note 3/Disable	High/Disable
MOD	Low/Disable	Low/Disable
$\overline{\text{OE}}$	High/Disable	High/Disable
PAR	Tristate/Disable	Tristate/Enable
PD[63:48]	High/Disable	Tristate/Disable
PD[47:32]	High/Disable	Tristate/Disable
PD[31:16]	High/Disable	Tristate/Disable
PD[15:0]	High/Disable	Tristate/Disable
PWM0	Driven/Disable	Driven/Disable
PWM1	Note 7/Disable	Tristate/Disable
RA[15:0]	High/Disable	Tristate/Disable
$\overline{\text{RAS}}$[1:0]	Note 2/Disable	High/Disable
RD[7:0]	High/Disable	Tristate/Disable
$\overline{\text{REQ}}$	Tristate/Disable	Tristate/Disable
$\overline{\text{RESET}}$	Input - Enable	Input - low
$\overline{\text{ROMEN}}$	Driven/Disable	High/Disable (Note 9)
RSET	Analog	Analog
SCLK	Input - Enable	Input - Enable
$\overline{\text{SDCAS}}$	High/Disable	High/Disable
SDCLK	Note 4/Disable	Tristate/Enable
SDCLKEN	Tristate/Disable	Tristate/Enable
SDCLKI	Input - Note 4	Input - Disable
$\overline{\text{SDRAS}}$	Note 2/Disable	High/Disable
SPCLK	Tristate/Disable	Tristate/Enable
SPDAT	Tristate/Disable	Tristate/Enable
STANDBY	Input - Enable	Input - Enable
$\overline{\text{STOP}}$	Tristate/Disable	Tristate/Enable
$\overline{\text{STWR}}$	Driven/Disable	Driven/Disable
SUSPEND	Input - Enable	Input - Enable
$\overline{\text{TRDY}}$	Tristate/Disable	Tristate/Enable
VCLK	Driven/Disable	Tristate/Enable
VREF	Analog	Analog
$\overline{\text{VREQ}}$/VRDY	High/Disable	Tristate/Enable
VS	Tristate/Disable	Tristate/Enable
VSYNC	Note 6/Disable	Tristate/Disable
$\overline{\text{WE}}$	High/Disable	High/Disable

XIN	Analog	Analog
XOUT	Analog	Analog

Notes:

1. Bidirectional pads have two states shown separated by a slash, i.e, Output state/Input state. For example, Tristate/Disable means the output buffer is tristated and the input buffer is disabled.
2. For EDO memory using self refresh, $\overline{\text{CAS}}$[7:0] and $\overline{\text{RAS}}$[1:0] stay low during Suspend. For 'SGRAM, CS[1:0], $\overline{\text{SDRAS}}$ and $\overline{\text{SDCAS}}$ are driven high during Suspend.
3. During Suspend, MA[10:0] retain the value prior to Suspend enable.
4. If CR6F_7 = 0, then the internal clock is used to latch data from the SGRAM/SDRAM. If CR6F_7 = 1, the SDCLKI input is used to latch the data.
5. The status of FPGPIO during Suspend is determined by SR35_3-0.
6. HSYNC and VSYNC are driven at the level they were driven prior to Suspend enable. SRD_7-4 can also be used to control the levels of these signals during Suspend.
7. If SR52_7 = 0, the ODD function is selected. The pin is tristated. If SR52_7 = 1, the PWM1 function is selected and the pin will be driven low.
8. SR32_0 = 1 tristates all memory interface signals.
9. FPPOL is selected when CR6F_0 = 1. The $\overline{\text{ROMEN}}$ function is selected when CR6F_0 = 0.

5.5 5V TOLERANCE

ViRGE/MX is a 3.3V device with 5V tolerance for the memory, CPU and LPB/CRT interfaces. If a 5V device is attached to a particular interface, a register bit must be set and the appropriate pin must be connected to 5V VDD as shown in Table 5-6.

Table 5-6. 5V Tolerance Setup

Interface	Register Bit (= 0 for 5V tolerance)	5V Tolerance Pin
Memory	SR1F_4	MEMTOL
CPU	SR1F_5	PCITOL
LPB/CRT	SR1F_6	LPBTOL

If a 5V tolerance pin is actually connected to 5V, the pads in the corresponding interface will consume a small static current. Therefore, to minimize power consumption, 5V tolerance pins must be connected to 3.3V if no 5V device is to be attached to that interface.

5.6 GREEN PC SUPPORT

ViRGE/MX provides support for the VESA Display Power Management Signaling (DPMS) protocol by allowing independent control of the HSYNC and VSYNC signals. To use this capability, the bit pattern xxxx0110b must be written to the SR8 register to unlock access to the SRD register. Bits 5-4 of SRD then control the state of HSYNC and bits 7-6 of SRD control the state of VSYNC.

If DCLK is stopped during Standby or Suspend, HSYNC and VSYNC become level. This may cause a problem when normal HSYNC/VSYNC operation is programmed (SRD_7-3 = 0000b). During Standby or Suspend, SR42_0 can be used to control the outputs on the HSYNC and VSYNC pins when SRD_7-3 = 0000b).

Section 6: PCI Interface

The pinout and other specifications for ViRGE/MX are in complete conformance with Revision 2.1 of the the PCI specification. No glue logic is required. Maximum SCLK for PCI bus operation is 33 MHz. PCI cycles at 66 MHz via an AGP bus are also supported. All connections, functions and timings are in conformance with the AGP 1.0 specification.

6.1 PCI CONFIGURATION

The Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Incorporated as the vendor. The Device ID register is hardwired to 8C01H.

Bits 10-9 of the Status register (Index 06H) are hardwired to 01b to specify medium $\overline{\text{DEVSEL}}$ timing. The Class Code register (Index 08H) is hardwired to 30000xxH to specify that ViRGE/MX is a VGA compatible device. Bits 3-0 of the Base Address 0 register (Index 10H) are hardwired to 00H. This indicates that the "prefetchable" bit is cleared to 0, the base register can be located anywhere in a 32-bit address space and the base register is located in memory space.

When ViRGE/MX powers up, it defaults to memory mapped I/O enabled at a relocatable base address of 7000 0000H. This allows the PCI system to reconfigure as required for plug and play.

6.2 PCI CONTROLS

ViRGE/MX provides several methods of controlling PCI Bus operation. PCI disconnects are enabled via CR66_3 and CR66_7. The RAMDAC snoop method is selected via CR34_0. PCI master abort handling during RAMDAC snooping can be disabled via CR34_1. PCI retry handling during RAMDAC snooping can be disabled via CR34_2. PCI read burst cycles can be disabled via CR3A_7.

6.3 PCI SUBSYSTEM ID

The Subsystem and Subsystem Vendor IDs are located in a 32-bit read only register at PCI2C. These registers reflect the content of 4 new read/write CR registers as follows:

Register	CR Space	PCI Configuration Space
Subsystem Vendor ID Low Byte	CR95	Index 2CH
Subsystem Vendor ID High Byte	CR96	Index 2DH
Subsystem ID Low Byte	CR97	Index 2EH
Subsystem ID High Byte	CR98	Index 2FH

These registers allow identification of particular vendors using the same graphics chip. The following design allows the subsystem identification to be handled by software (no hardwiring).

For add-in card cases, the system BIOS will typically attempt to read the subsystem ID information before the video BIOS is run. When this occurs, ViRGE/MX will check a read/write Subsystem ID Source bit (CR37_2), which defaults to 1 on power-up. This bit is defined as follows:

CR37_2 - Subsystem ID Source

0 = Read subsystem ID information from chip registers
1 = Read subsystem ID information from BIOS

On power-up, with this bit set to 1, the following occurs:

1. The PCI bus is claimed and held by ViRGE/MX when an attempt to read the subsystem ID occurs.
2. Video ROM BIOS locations C0040-C0043 are read, depending on which $\overline{\text{BE[0:3]}}$ lines are enabled. For example, if only $\overline{\text{BE0}}$ is enabled, then the byte at C0040 will be read. The information in C0040-C0043 is editable using S3's Video BIOS edit utility, and thus can be tailored by each vendor. The ROM information is automatically copied into the ID registers (CR95-CR98 and the mirrored PCI2C-PCI2F).
3. The PCI bus is released.
4. (Some time later) The video BIOS is run. It resets CR37_2 to 0. Until this step is taken, all subsystem register accesses will generate the sequence listed in steps 1-3 above.

From this point on until the next hard re-boot, all subsystem register accesses will be directed to the PCI subsystem registers. A soft reset (e.g., CTL-ALT-DEL) does not change the state of CR37_2 and thus does not affect the subsystem ID read process.

Motherboard designs incorporate the video BIOS and system BIOS in the same ROM, so care must be taken that ViRGE/MX does not generate a video ROM access cycle. To accomplish this, PD10 is pulled low at reset to latch a 0 in CR37_2. The system BIOS must then load the subsystem ID information in ViRGE/MX before any ID scanning takes place. To do this, it must turn on ViRGE/MX, enable I/O accesses in the PCI configuration space, unlock the CR registers, program the subsystem ID information in the registers described above, then turn off ViRGE/MX.

6.4 PCI POWER MANAGEMENT

PCI04_4 is hardwired to 1 to indicate a capabilities list is available. PCI34_7-0 point the the PCI power management registers starting at offset DC. The basic power states (D0-D3) are supported are supported as explained by the PCI Bus Power Management Interface Specification, Revision 1.0. ViRGE/MX also provides the maintaining clock capability as defined by the *PCI Mobile Design Guide*, Revision 1.0. The $\overline{\text{CLKRUN}}$ pin (U13) supports this function. See the above referenced design guide for a complete description of this function and its specifications.

Section 7: Display Memory

ViRGE/MX supports either EDO DRAM, SDRAM or SGRAM for its video frame buffer. For each type of memory, this section describes the various configurations supported, the functional timing for memory accesses and the operation of various register bits that affect memory timing and operation.

7.1 EDO MEMORY SUPPORT

ViRGE/MX requires EDO memory capable of 1-cycle operation. Bits 3-2 of CR36 are set to 01b to indicate that 1-cycle EDO DRAM operation is being used.

Supported EDO DRAM features are:

- 66 MHz MCLK, 1-cycle operation (528MB/sec. peak graphics bandwidth in a x64 configuration)
- 1-cycle operation
- Self refresh mode
- Slow refresh mode (8 mS, 16 mS, 64 mS)

7.1.1 EDO Memory Configurations

ViRGE/MX supports a 2- or 4- MByte EDO DRAM configuration. Supported memory types are:

- 256Kx16 EDO
- 512Kx32 EDO (86C261 only)

Figure 7-1 shows the signal connections when using 256Kx16 DRAMs. Figures 7-2 provides the same information for 512Kx32 DRAMs. The video BIOS determines the memory size at boot time and programs it in CR36_7-6.

7.1.2 EDO Memory Refresh

ViRGE/MX supports several EDO DRAM refresh methods. For normal operation, it uses the standard $\overline{CAS}$ before $\overline{RAS}$ method. The functional timing for this can be found in any standard DRAM data book.

Refresh can be done during the horizontal blanking time (CR74_0 = 1) or distributed (CR74_0 = 0). For either case, the frequency of refreshes is specified via CR75_7-0.

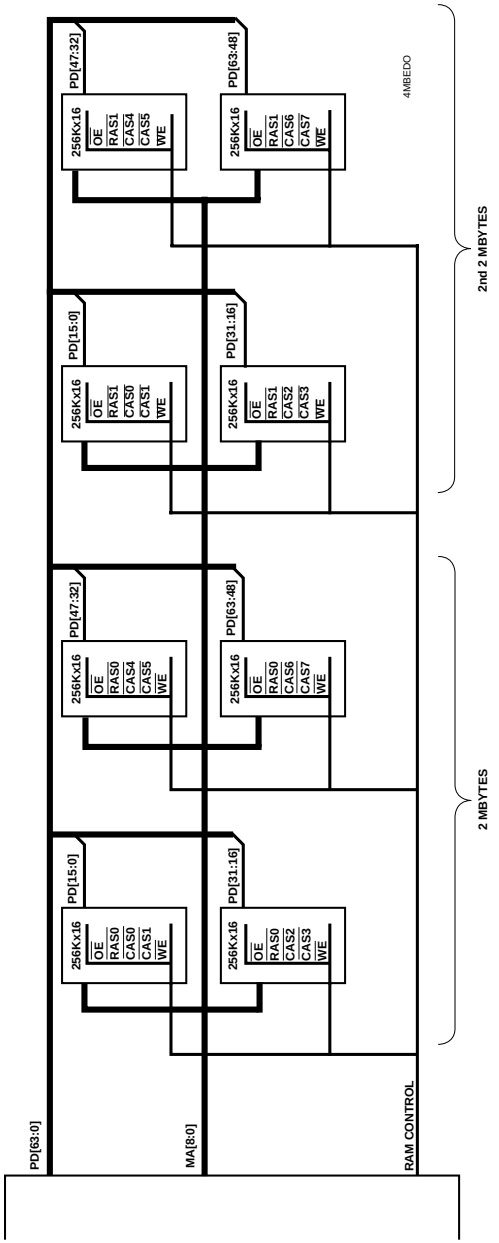


Figure 7-1. 256Kx16 EDO DRAM Configurations

During power saving modes, ViRGE/MX supports slow refresh based on the 32 kHz clock or self-refresh, assuming the DRAMs can support these. The desired selection is made via SR74_3-1 as follows:

000 = Self refresh
100 = Normal (8 ms)
101 = 16 ms slow refresh
110 = 64 ms slow refresh
111 = 128 ms slow refresh

If self refresh is selected, burst refreshes can be enabled before and after the self refresh via CR74_4 and CR74_5.

The BIOS needs to be aware of the DRAM capabilities and set these bits appropriately.

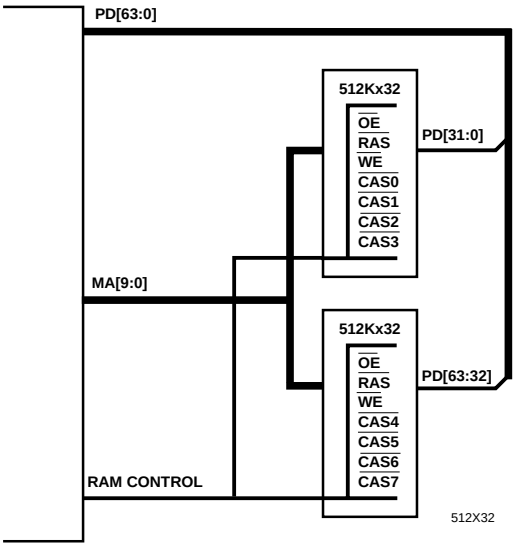


Figure 7-2. 512Kx32 EDO DRAM Configurations

7.1.3 EDO Memory Functional Timing

Figure 7-3 shows the functional timing for a 1-cycle EDO read cycle. This also shows how certain parameters for various control signals can be adjusted to meet the access time requirements of a variety of DRAMs. The settings in CR68 and CR6F can be made by power-on strapping of the appropriate PD pins at reset. All settings can be changed by programming after reset.

The DRAM drives valid read data after the $\overline{CAS}$ falling edge at T5. The chip latches the data on the next falling $\overline{CAS}$ edge. Note that a dummy cycle is required at the end to latch the last read.

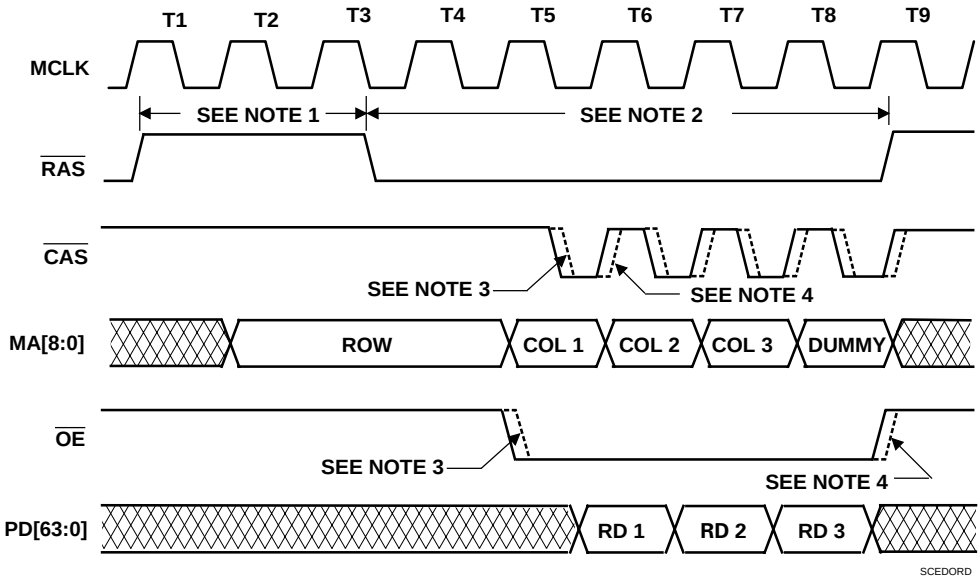


Figure 7-3. 1-cycle EDO Read Cycle

Notes

1. The $\overline{RAS}$ precharge time can be adjusted from 1.5 to 3.5 MCLKs via CR68_5-4 and reduced by 0.5 MCLK via CR78_0.
2. The minimum $\overline{RAS}$ low time for the first column access can be adjusted from 2.5 to 3.5 MCLKs via CR68_3
3. $\overline{CAS}$ and $\overline{OE}$ falling edges can be stretched via CR68_1-0 and CR6F_6-5 respectively if CR68_2 = 1.
4. $\overline{CAS}$ and $\overline{OE}$ rising edges can be stretched via CR68_1-0 and CR6F_6-5 respectively if CR68_2 = 0.

Figure 7-4 shows the functional timing for a 1-cycle EDO write cycle. Write data is latched by the DRAM on the falling edge of $\overline{CAS}$. No dummy cycle is required.

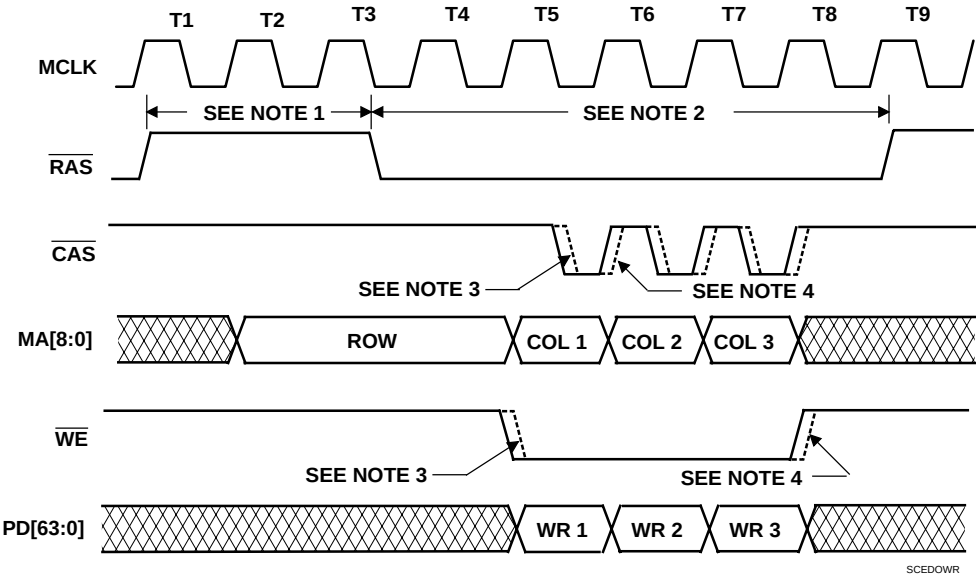


Figure 7-4. 1-cycle EDO Write Cycle

Notes

1. The $\overline{RAS}$ precharge time can be adjusted from 1.5 to 3.5 MCLKs via CR68_5-4 and reduced by 0.5 MCLK via CR78_0.
2. The minimum $\overline{RAS}$ low time for the first column access can be adjusted from 2.5 to 3.5 MCLKs via CR68_3
3. $\overline{CAS}$ and $\overline{WE}$ falling edges can be stretched via CR68_1-0 and CR6F_4-3 respectively if CR68_2 = 1.
4. $\overline{CAS}$ and $\overline{WE}$ rising edges can be stretched via CR68_1-0 and CR6F_4-3 respectively if CR68_2 = 0.

Figure 7-5 shows the functional timing for a 1-cycle EDO read/write cycle. A dummy cycle is added between the read and write.

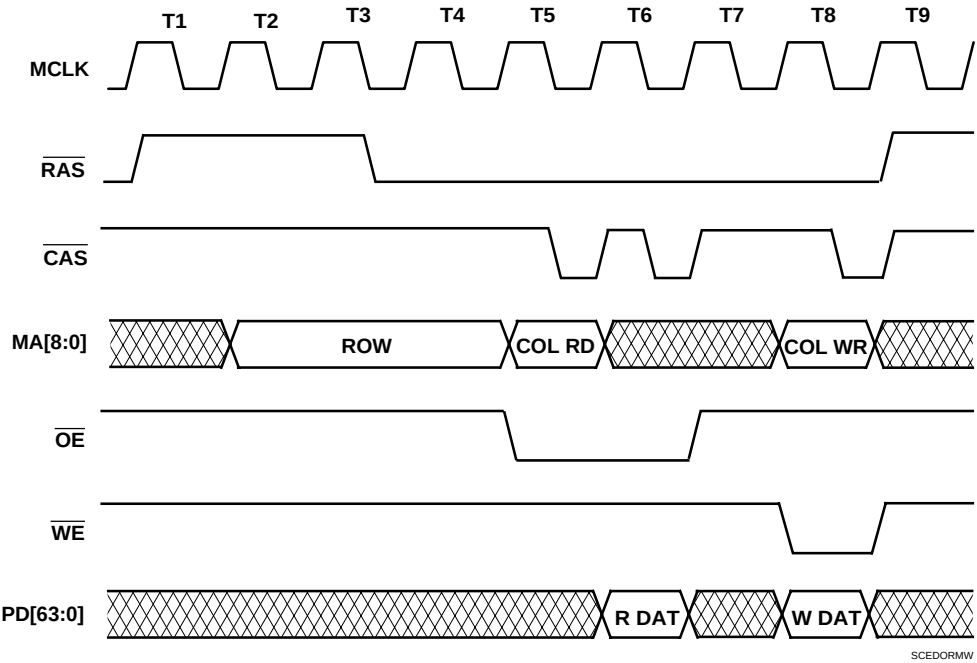


Figure 7-5. 1-cycle EDO Read/Write Cycle

7.2 SDRAM/SGRAM SUPPORT

CR36_3-2 are programmed via power-on strapping to 11b to indicate that SDRAM/SGRAM is used for the frame buffer.

Supported SDRAM/SGRAM features are:

- 83 MHz MCLK (640 MBytes/sec. peak graphics bandwidth)
- Mode register set
- Self refresh
- Auto refresh
- Precharge all banks
- Bank active
- Device deselect
- Power down
- Burst read of size 1
- Burst write of size 1

7.2.1 SDRAM/SGRAM Configurations

ViRGE/MX supports 2- or 4- MByte SDRAM/SGRAM configuration. Supported memory types are:

- 256Kx16 SDRAM
- 256Kx32 SGRAM
- 512Kx32 SGRAM (86C261 only)

Figure 7-6 shows the signal connections for SDRAM configurations. Figures 7-7 and 7-8 show the supported SGRAM configurations. The video BIOS determines the memory size at boot time and programs it in CR36_7-6.

7.2.2 SDRAM/SGRAM Mode Set

SDRAMs/SGRAMs require that their operating mode be programmed after reset. The $\overline{CAS}$ latency is programmed via power-on strapping and is latched in CR6F_6-5. This setting is written to the SDRAM/SGRAM by a mode set cycle generated when CR72_5 is set to 1.

7.2.3 SDRAM/SGRAM Refresh

ViRGE/MX supports two SDRAM/SGRAM refresh methods. For normal operation, it uses auto refresh (the standard $\overline{CAS}$ before $\overline{RAS}$ method). The functional timing for this can be found in any SDRAM/SGRAM data book. The time from the last refresh cycle to the next activate command is programmable via CR68_1-0.

Refreshing can be done during the horizontal blanking time (CR74_0 = 1) or distributed (CR74_0 = 0). For either case, the frequency of refreshes is specified via CR75_7-0.

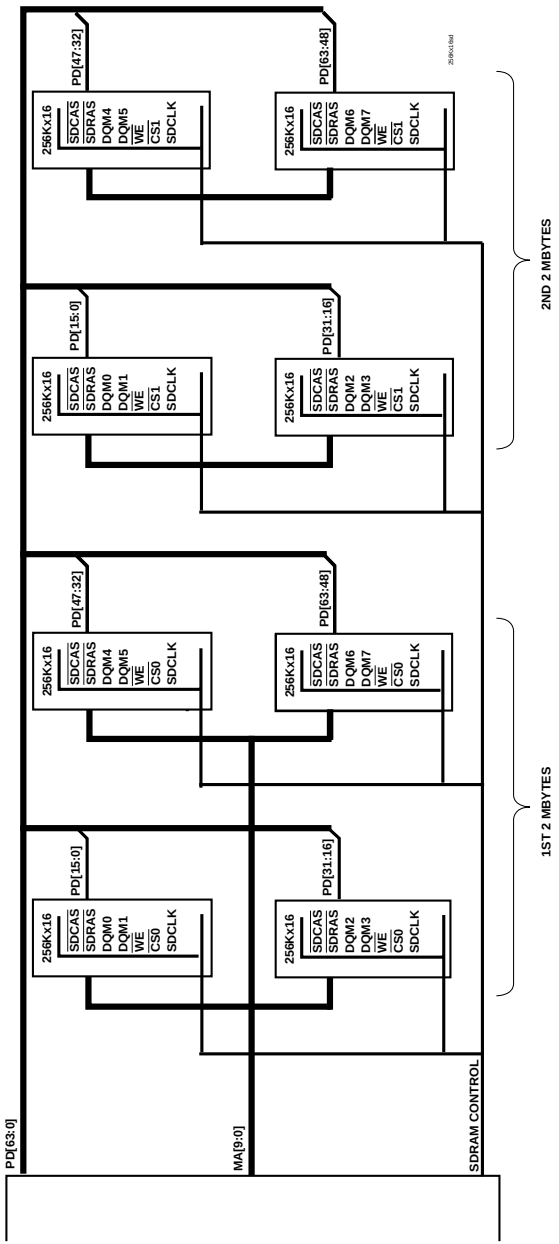


Figure 7-6. 256Kx16 SDRAM Configurations

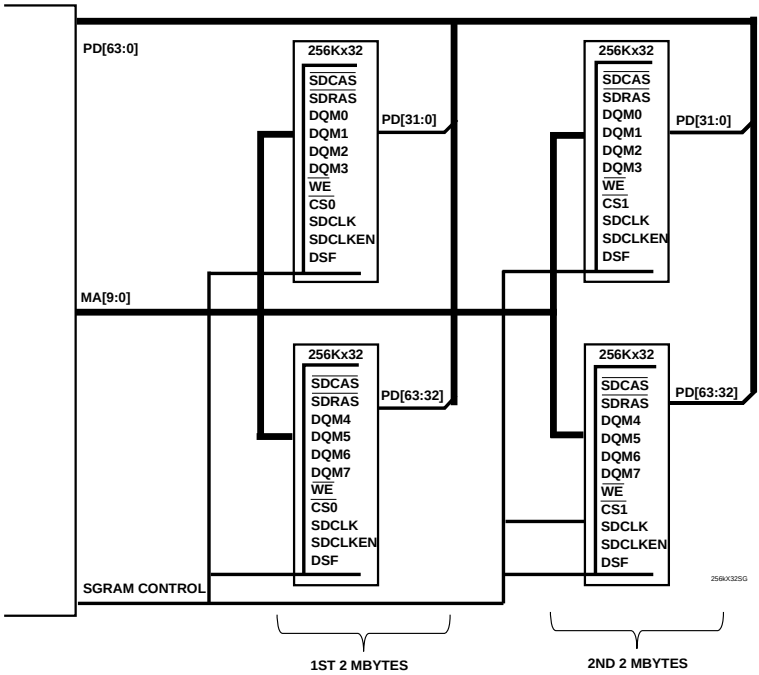


Figure 7-7. 256Kx32 SGRAM Configurations

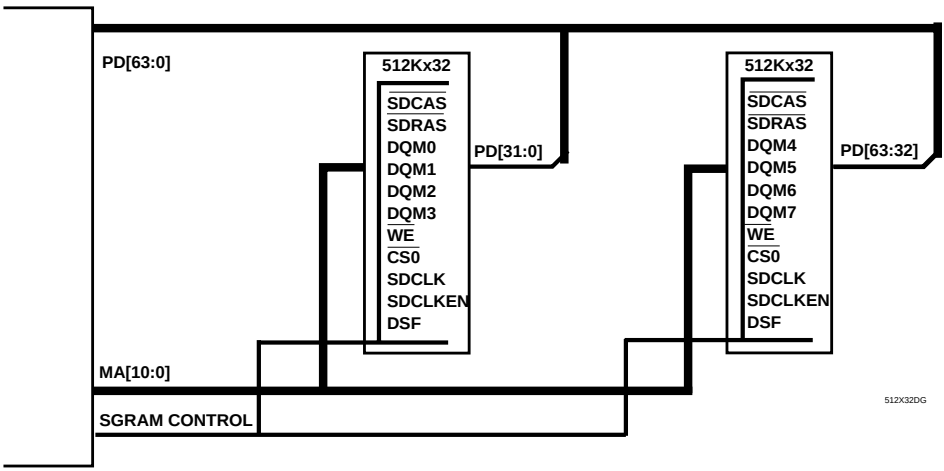


Figure 7-8. 512Kx32 SGRAM Configurations

During power saving modes, ViRGE/MX supports self-refresh or power down. The desired selection is made via SR74_3-1 as follows:

000 = Self refresh
001 = Power down

If self refresh is selected, burst refreshes can be enabled before and after the self refresh via CR74_4 and CR74_5. If power down mode is selected, display memory data will be lost and must be re-written upon power up.

7.2.4 SDRAM/SGRAM Read Data Latching

When CR6F_7 = 0, latching of read data is based on an internal clock. When CR6F_7 = 1, latching of read data is based on the input to the SDCLKI pin. This signal is a loopback of the SDCLK output. The SDCLK line is tapped such that the SDCLKI trace length is equal to the average of the longest and shortest PD line traces. Use of the SDCLKI pin is recommended for MCLK > 66 MHz.

7.2.5 SDRAM/SGRAM Functional Timing

This section provides functional timing for SDRAM/SGRAM read and write cycles and describes how certain timing parameters can be adjusted via power-on strapping or register programming.

Figure 7-9 shows the functional timing for an SDRAM/SGRAM read cycle. COMMAND is made up by a standard combination of CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. DSF is not used, meaning that SGRAMs function identically to SDRAMs. Please refer to SGRAM data sheets for the truth table. Illustrated in the figure is a sequence of 4 reads of burst length 1. Before any READ or WRITE commands can be issued to a bank within the SGRAM, a row in that bank must be “opened”. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated. A read is then initiated with a READ command, as illustrated. Illustrated in Figure 7-9 is the relative timing of the feedback clock, SDCLKI, with the data at the PD inputs. SDCLKI is used to provide adequate setup and hold times for reads when the SDCLK frequency is greater than 66 MHz.

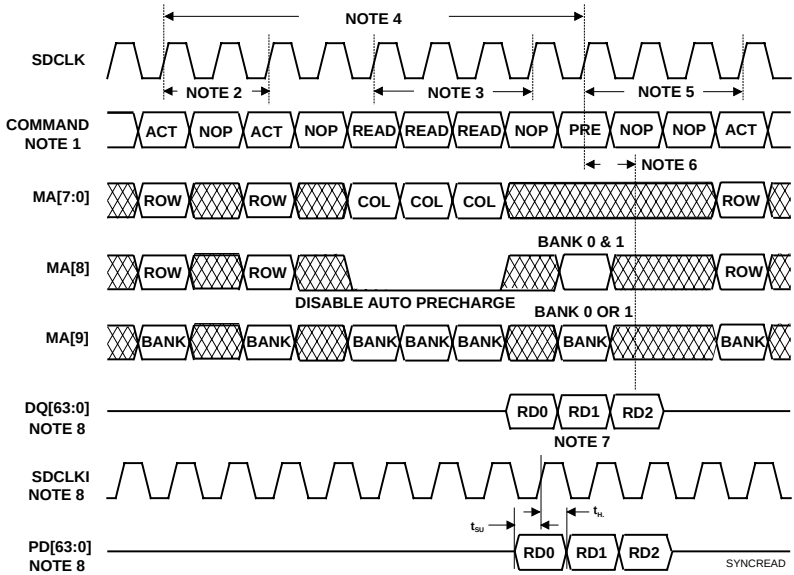


Figure 7-9. SDRAM/SGRAM Read Cycle - CAS Latency 3

Notes:

1. SDRAM/SGRAM data sheets provide the command truth tables.
2. Consecutive bank activation timing is programmed via CR6F_3.
3. $\overline{CAS}$ latency is programmable via CR6F_6-5.
4. Minimum $\overline{RAS}$ active to the next $\overline{RAS}$ precharge time (t_{RAS}) is programmable via CR68_3.
5. $\overline{RAS}$ precharge time (t_{RP})is programmable via CR68_5-4.
6. The last data out to row precharge delay is programmable via CR6F_4. This is only effective if the minimum t_{RAS} time restriction is met.
7. Burst length is fixed at 1.
8. DQ is data at the SDRAM/SGRAM output pins. PD is data at ViRGE/MX input pins. SDCLKI is used to latch the read data if CR6F_7 = 1.

Figure 7-10 shows the functional timing for a sequence of 4 SDRAM/SGRAM write cycles (burst = 1). The first WRITE command is issued t_{RCD} clock cycles after the ACTIVE command. The bank and row addresses are asserted during ACTIVE. The column and bank addresses are provided with each WRITE command. Valid data is output coincident with each WRITE command.

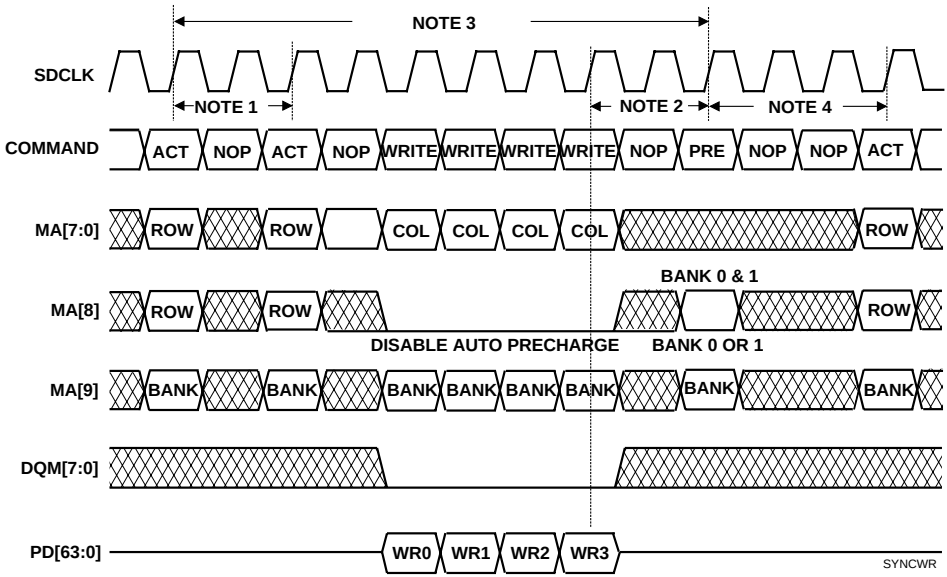


Figure 7-10. SDRAM/SGRAM Write Cycle

Notes:

1. Consecutive bank activation timing is programmed via CR6F_3.
2. Last data in to row precharge delay is programmable via CR68_2.
3. Minimum $\overline{RAS}$ active to the next $\overline{RAS}$ precharge time (t_{RAS}) is programmable via CR68_3.
4. $\overline{RAS}$ precharge time (t_{RP})is programmable via CR68_5-4.

Section 8: Clock Synthesis and Control

ViRGE/MX contains three phase-locked loop (PLL) frequency synthesizers. These generate the DCLK1 and DCLK2 (video clocks) and MCLK (memory clock) signals.

8.1 CLOCK SYNTHESIS

Each PLL scales a single reference frequency input on the XIN pin. By placing a parallel-resonant crystal between the XOUT output pin and the XIN pin, the reference frequency is generated by the internal oscillator. Alternately, a CMOS-compatible clock input can be connected to XIN to provide the reference frequency.

The frequency synthesized by each PLL is determined by the following equation:

$$f_{OUT} = \frac{(M+2)}{(N+2)\times 2^{R}} \times f_{REF}$$

Programmed PLL M and PLL N values should be consistent with the following constraint:

$$170MHz \leq \frac{(M+2)f_{REF}}{(N+2)} \leq 340MHz$$

Note that values used for the parameters are the integer equivalents of the programmed values.

There are five pairs of PLL programming registers. One pair specifies the MCLK frequency. Normally, two pairs specify the DCLK1 and DCLK2 frequencies in VGA modes and two other pairs specify these frequencies in Enhanced modes. The exceptions will be noted later.

The resolutions of the synthesizers depend on the number of bits available to specify each parameter. Enhanced mode DCLK2 is programmed via SRE and SRF. It has the highest resolution, with the following bit ranges: M = 9, N = 7, R = 3. Enhanced Mode DCLK1 is programmed via SR12 and SR13. Its bit ranges are: M = 7, N = 5, R = 3. The two VGA DCLKs are programmed via SR22-SR25. Their bit ranges are: M = 7, N = 5, R = 2. MCLK is programmed via SR10 and SR11, with the same resolution as the VGA DCLKs. Overflow bits for these bit ranges are found in SR29.

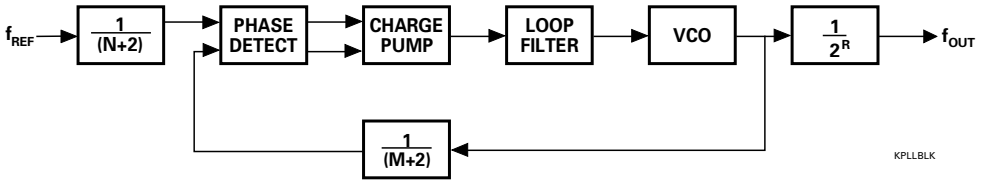


Figure 8-1. PLL Block Diagram

The PLL feedback loop frequency from the voltage controlled oscillator stage is scaled by dividing that frequency by (M+2). The reference frequency is divided by (N+2) before being fed to the phase detector stage of the PLL.

The PLL R value codes the selection of a frequency divider for the PLL output. This is shown Table 8-1. Note that only the Enhanced mode DCLKs have a 3-bit range; the others use the 2 lsb's of the range code with a maximum divider of 8.

Table 8-1. PLL R Parameter Decoding

R-Range Code	Frequency Divider
000	1
001	2
010	4
011	8
100	16

The entire PLL block diagram is shown in Figure 8-1.

The following sequence may be followed to arrive at M and N values for any mode.

1. Calculate an R which does not violate the following constrains:

   $$170MHz < 2^R \times f_{OUT} \leq 340MHz$$

2. Start with N1 = 1 and calculate:

   $$M = [\frac{f_{OUT} \times (N+2) \times 2^R}{f_{REF}}] - 2$$

3. Determine if the following constraint is met:

   $$0.995\ f_{OUT} < \frac{(M+2)\ f_{REF}}{(N+2)\ 2^R} < 1.005\ f_{OUT}$$

4. If the constraint in step 3 is met, the M and N values used will generate the desired frequency (within the specified tolerance). If the constrain is not met, repeat steps 2 and 3 with N increased by 1 each time until the constraint in step 3 is met. Note that multiple combinations of M and N are possible for a given output frequency.

8.2 CLOCK SELECTION AND REPROGRAMMING

ViRGE/MX has two graphics controllers. The Controller 1 DCLK is selected via SR30_3 (0 = DCLK1, 1 = DCLK2). The Controller 2 DCLK is selected via SR30_4 (0 = DCLK2, 1 = DCLK1). Note that by default, Controller 1 is assigned DCLK1 and Controller 2 is assigned DCLK2.

The decision as to which DCLK to assign to which controller is influenced by several factors. It may be necessary, for example, to assign DCLK2 (highest resolution) to the controller driving the output with the highest frequency accuracy requirement (e.g.,, TV).

The foremost factor is whether the graphics mode is VGA or Enhanced. Only Controller 1 can be used for a VGA mode. If the DCLK driving it (either DCLK1 or DCLK2) is only driving Controller 1, then for VGA modes, the source for the PLL parameter values is specified by 3C2H_3-2. If 3C2H_3-2 = 00b, the DCLK PLL parameters are taken from SR22 and SR23. The default values generate a frequency of 25.175 MHz. This is the DCLK frequency generated at power on to support standard VGA operation. If 3C2_3-2 = 01b, the DCLK PLL parameters are taken from SR24 and SR25. The default values generate a frequency of 28.322 MHz.

If the same DCLK is driving both Controller 1 and Controller 2, 3C2H_3-2 are ignored and the PLL parameter values are taken from SR12 and SR13 for DCLK1 and from SRE and SRF for DCLK2. This is also the case for 3C2H_3-2 = 11, which is the setting for all Enhanced modes. This can also be forced by setting SR1B_7 to 1. No default values are defined for these PLL registers.

New DCLK PLL parameter values can be programmed at any time. They can be loaded in one of two ways. If bit 5 of SR15 is cleared to 0, the new DCLK frequency is loaded by setting bit 1 of SR15 to 1. Bit 1 of SR15 should be left at a value of 1. Actual loading will be delayed for a short but variable period of time.

The alternate approach to loading the new DCLK frequency is to toggle bit 5 of SR15 by programming it to a 1 and then a 0. This immediately loads the DCLK (and MCLK} frequencies (no variable delay). For example, pseudocode to change DCLK to the frequency specified by PLL parameter values of 34H and 56H is:

```
3C2 ⇐ 6FH                ; DCLK specified by
                         ; SR12 and SR13
3C4 ⇐ 12H                ; SR12 index
3C5 ⇐ 34H                ; SR12 PLL value
3C4 ⇐ 13H                ; SR13 index
3C5 ⇐ 56H                ; SR13 PLL value
3C4 ⇐ 15H                ; SR15 index
3C5 ⇐ RMW                ; Use read/modify/write to
                         ; set bit 5 to 1 and leave
                         ; other bits unchanged
3C5 ⇐ RMW                ; Use read/modify/write to
                         ; clear bit 5 to 0 and
                         ; leave other bits
                         ; unchanged
```

Either loading approach should work. The second (immediate loading) approach helps with system testing since the timing of the load is predictable. The first approach (via bit 1 of SR15) has the advantage of separating the loading of DCLK from that of MCLK.

After power-up, all MCLK frequency changes must be made by re-programming SR10 and SR11. If bit 5 of SR15 is cleared to 0, the new frequency does not take effect until a 1 has been written to bit 0 of SR15. This bit must then be cleared to 0 to prevent repeated loading. Actual loading will be delayed for a short but variable period of time.

As explained above for DCLK, toggling bit 5 of SR15 (0,1,0) immediately loads both the DCLK values in the register pair selected by 3C2H_3-2 and the MCLK values in SR10 and SR11.

8.3 CLOCK CONTROL

In clock doubled mode (CR67_7-4 = 0001b), the internal RAMDAC requires two clocks. The normal internal DCLK frequency is divided by two via SR15_4 = 1 (DCLK1) or SRB_4 = 1 (DCLK2) to provide the standard pixel clock input. Undivided DCLK provides the other input. This clock can be inverted via SR15_6 = 1 (DCLK1) or SRB_6 = 1 (DCLK2).

Certain 4 bits/pixel modes require that DCLK be halved. This is done with bit 6 of AR10 set to 1 and bit 4 of CR3A cleared to 0 and is enabled by setting SR15_4 to 1 (DCLK1) or SRB_4 = 1 (DCLK2).

8.4 CLOCK TESTING

The procedure for testing clock synthesis is:

1. Program SR10/SR11 (MCLK) or SR12/SR13 or SRE/SRF (DCLK) to generate the desired frequency.
2. Select either MCLK or one of the DCLKs for testing via SR14_3 and SRB_3. If a DCLK is selected, also ensure that 3C2H_3-2 = 11b to select SR12/SR13 or SRE/SRF as the source of the DCLK PLL parameters.
3. Clear the clock synthesizer counter by toggling SR14_4.
4. Set SR14_2 = 1 for some exact amount of time (Δt).
5. Read SR16 (most significant byte) and SR17 (least significant byte). This is the binary count of the number of clock cycles actually executed.
6. Calculate the expected result (Δt/clock period) and compare it with the value read in the previous step. The two should agree within 2 or 3 counts.

Section 9: Streams Processor

The S3 Streams Processor processes data from the graphics frame buffer, composes it and outputs the result to the internal DACs for generation of the analog RGB outputs to the monitor. The general data flow is shown in Figure 9-1. Note that the DAC shown in this figure is inside ViRGE/MX.

9.1 INPUT STREAMS

The processor can compose data from up to 4 independent streams as shown in Figure 9-1.

1. Primary Stream - RGB graphics data
2. Secondary Stream - RGB or YUV/YCbCr (video) data from another region within the frame buffer
3. Hardware Icon - 64x64x4 (or 128x128x2)
4. Hardware Cursor - 64x64x2 cursor

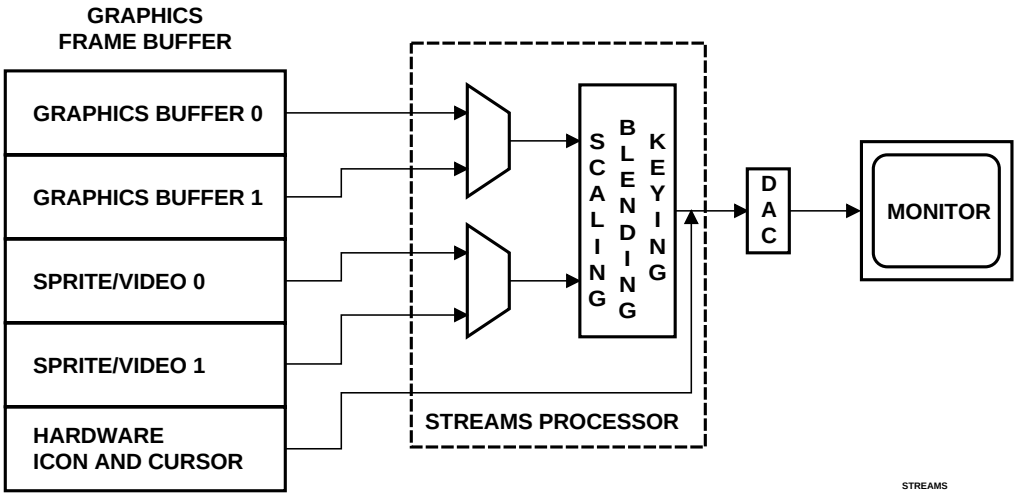


Figure 9-1. Streams Processor

Regardless of the input formats, the Streams Processor creates a composite RGB-24 (8.8.8) output to the DACs. This means that, for example, RGB-8 pseudo-color graphics data can be overlaid with true-color-equivalent (24 bits/pixel) video data. The result is improved video quality and/or reduced memory bandwidth requirements as compared with systems that require both graphics and video to be stored in the same frame buffer format. In certain modes, the Streams Processor also saves memory bandwidth by eliminating the need to save and restore the overlay background since the background (primary stream) is never overwritten in the frame buffer.

Streams Processor support is not available for clock-doubled 8 bits/pixel modes, interlaced graphics modes and standard VGA modes except for modes D, E, 10, 12 and 13.

Streams Processor operation is enabled by CR67_2 = 1. This must only be done during the vertical blanking period. If CR67_3 = 0, standard VGA registers (CRC and CRD, with extension in CR69) are used to control the primary stream frame buffer address. If CR67_3 = 1, the primary stream frame buffer address is specified via MM81C0, MM81C4 and MM81CC_0

9.1.1 Primary Stream Input

The primary stream is generated by reading the RGB pixel data written to the frame buffer by the graphics controller. The format for this data can be any of the following as selected via CR67_7-4.

- RGB-4 or 8
- KRGB-16 (1.5.5.5) - The K bit can be used for alpha keying
- RGB-16 (5.6.5)
- RGB-24 (8.8.8) - packed
- XRGB-32 (X.8.8.8) - X can be used for 8-bit alpha keying (MM8184_30-29 = 01b). This mode is not supported by the graphics engine.

9.1.2 Secondary Stream Input

The secondary stream is generated by reading pixel data from a separate section of the frame buffer than that used to generate the primary screen. This might be RGB data written by the graphics controller, such as a sprite used by game programmers for moving objects. It could also be RGB, YUV or YCbCr data written to the frame buffer by some video source (CPU, decoder, digitizer). The format for this data can be any of the following as selected via bits 26-24 of MM8190.

- YCbCr-16 (4.2.2), 16 to 240 input range
- YUV-16 (4.2.2), -128 to 127 input range
- KRGB-16 (1.5.5.5) - The K bit is the color key.
- YUV (2.1.1)
- RGB-16 (5.6.5)
- RGB-24 (8.8.8)
- XRGB-32 (X.8.8.8) - X is the ignored upper byte except with 8-bit alpha keying (MM8184_30-29 = 01b). This mode is not supported by the graphics engine.

The data can be passed through unscaled or scaled up horizontally and vertically by an arbitrary amount. YCbCr/YUV data is color space converted and all data is converted to RGB-24 (8.8.8) format.

9.1.3 Hardware Icon and Cursor Generation

Hardware icon and cursor generation is explained in Section 15. The icon overlays everything but the cursor. The cursor overlays all other image sources.

9.1.4 Frame Buffer Organization/Double Buffering

For each stream to be used, the starting location (offset) in the frame buffer and the stride (byte offset between vertically adjacent pixels on the screen) must be specified. Both the primary and the secondary streams can be double buffered as depicted in Figure 9-1. This means that duplicate frame buffer storage can be provided for both the primary and secondary image (or for either one of them). With double buffering, the programmer can rapidly switch from one primary or secondary image to the other. In addition, having two images allows more time for updating one image while the other is being displayed. Defining the frame buffer organization and implementing double buffering are done via the register fields described in Table 9-1. For primary stream double buffering, the buffer being displayed is selected via the VGA display start address registers (CRC, CRD). LPB stands for Local Peripheral Bus. LPB stands for Local Peripheral Bus.

Table 9-1. Register Fields Used For Specifying Frame Buffer Organization and Double Buffering

Register Field	Description
MM81CC_2-1	Secondary Stream Buffer Select 00 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream 01 = Secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream 10 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input stream. Which alternative applies is determined by LPB starting address register selected by bit 4 of this register. 11 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF0C_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF10_21-0) used for the LPB input stream. Which alternative applies is determined by the LPB starting address register selected by bit 4 of this register.
MM81CC_4	LPB Input Buffer Select 0 = LPB frame buffer starting address 0 (MMFF0C_21-0) used for LPB input 1 = LPB frame buffer starting address 1 (MMFF10_21-0) used for LPB input
MM81CC_5	LPB Input Buffer Select Loading 0 = The value programmed in bit 4 of this register takes effect immediately 1 = The value programmed in bit 4 of this register takes effect at the end of the next frame (completion of writing all the data for a frame into the frame buffer)

Table 9-1. Register Fields Used For Specifying Frame Buffer Organization and Double Buffering (continued)

Register Field	Description
MM81CC_6	LPB Input Buffer Select Toggle 0 = End of frame (completion of writing all the data fro a from into the frame buffer) has no effect on the setting of bit 4 of this register 1 = End of frame causes the setting of bit 4 of this register to toggle
MM81E8_28	DDA Vertical Accumulator Initial Value Select 0 = Use only DDA Vertical Accumulator Initial Value 0 1 = Use both DDA Vertical Accumulator Initial Values 0 and 1
MM81D0_21-0	Secondary Display Buffer Address 0. This is the starting address (offset) in the frame buffer for 1 secondary graphics or video image.
MM81D4_21-0	Secondary Display Buffer Address 1. This is the starting address (offset) in the frame buffer for a second secondary graphics or video image.
MM81D8_11-0	Secondary Stream Stride. This is the byte offset in the frame buffer from a pixel in a given secondary image display line to the pixel directly below it on the next display line. The stride must be the same for both secondary buffers.
MMFF0C_21-0	LPB Frame Buffer Address 0. This is the starting address (offset) in the frame buffer for one image buffer into which is written data from the LPB. The secondary stream can be generated from this buffer.
MMFF10_21-0	LPB Frame Buffer Address 1. This is the starting address (offset) in the frame buffer for a second image buffer into which is written data from the LPB. The secondary stream can be generated from this buffer.

The secondary stream can be generated from data written to the frame buffer via the LPB when LPB mode is enabled. In this case, the Secondary Display Buffer Address 0 and the LPB Frame Buffer Address 0 will normally be the same, as will the Address 1's for both the secondary stream and the LPB input if double buffering is used. The various LPB control bits described in Table 9-1 allow complete hardware control of the capture and display of video data using either single or double buffering.

9.2 INPUT PROCESSING

Different processing options are available for the primary and secondary input streams. These are explained next.

9.2.1 Primary Stream Processing

The primary stream input RGB format is converted to RGB-24 (8.8.8) format. Each color byte is padded as required with low order zeros. After this conversion, the data is displayed using the CRT control registers. The primary stream always occupies the entire active screen and is the background window.

9.2.2 Secondary Stream Processing

The secondary stream input format is converted (if required) to RGB-24 (8.8.8) format. For YUV/YCbCr inputs, the required color space conversion is automatically performed. Before conversion, the data can be passed through unscaled or scaled up horizontally and/or vertically by arbitrary factors. Horizontal scaling uses interpolation. Vertical scaling uses line replication (MM81E8_15 = 0) or interpolation (MM81E8_15 = 1). Note that vertical interpolation cannot be used if 3-line flicker filter

mode is enabled (SR70_1-0 = 01b). The register fields involved in scaling up the secondary stream are described in Table 9-2. Figure 9-2 graphically describes the various fields.

For example, assume a 10x10 window that is to be scaled up horizontally by a factor of 2.5. The filter characteristics are set for bi-linear (2x to 4x stretch). The starting line width is 10 pixels and the ending line width is 25 pixels. The DDA horizontal accumulator initial value is 2 (10-1) - (25-1) = -6. The K1 horizontal factor is 10-1 = 9. The K2 horizontal factor is 10-25 = -15. Programming these parameters with these values results in a 2.5x horizontal stretch for the secondary stream window.

MM81E8_14 = 1 enables a bandwidth saving feature when interpolation is used for secondary stream scaling.

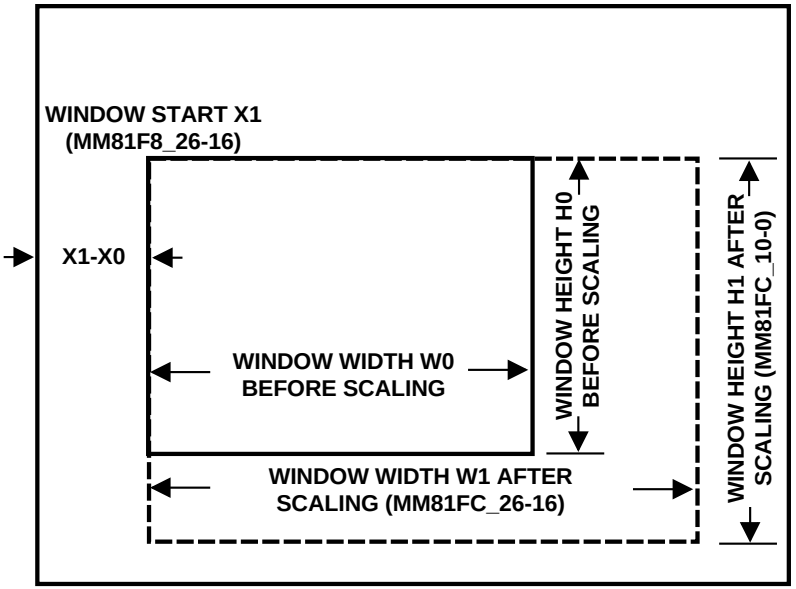


Figure 9-2. Screen Definition Parameters

Table 9-2. Register Fields Used For Scaling Up the Secondary Stream

Register Field	Description
MM8190_11-0	DDA Horizontal Accumulator Initial Value. Value = 2 (W0-1) - (W1-1), where W0 is the line width in pixels before scaling and W1 is the line width after scaling. This is a signed value.
MM8190_23	Secondary Stream Horizontal Filter Disable 0 = No effect 1 = Horizontal filter disabled when there is a secondary key match
MM8190_30-28	Filter Characteristics 000 = Secondary stream (pass-through) 001 = Secondary stream, linear, 0-2-4-2-0, for X stretch 010 = Secondary stream, bi-linear, for 2X to 4X stretch 011 = Secondary stream, linear, 1-2-2-2-1, for 4X stretch This selection applies only to horizontal scaling.
MM8198_10-0,	K1 Horizontal Factor. Value = W0-1, where W0 is the line width in pixels before scaling. This is a signed value.
MM8198_26-16	K2 Horizontal Factor. Value = W0-W1, where W0 is the line width in pixels before scaling and W1 is the line width after scaling. This is a signed value.
MM81E0_10-0,	K1 Vertical Factor. Value = [height (in lines) of the initial output window (before scaling)] -1. The initial output window height is the vertical resolution of the data written to the frame buffer and is shown as H0 in Figure 9-2.
MM81E4_10-0,	K2 Vertical Factor. Value = [height (in lines) of the initial output window (before scaling)] - [height (in lines) of the final output window (after scaling)] The initial output window height is the vertical resolution of the data written to the frame buffer and is shown as H0 in Figure 9-2. The final value is shown as H1 in Figure 9-2.
MM81E8_11-0,	DDA Vertical Accumulator Initial Value 0. Value = [height (in lines) of the output window after scaling] -1. This is shown as H1 in Figure 9-2. This value is used when MM81E8_28 = 0. If MM81E8_28 = 1, this value is used only when the secondary stream comes from secondary buffer 0.
MM81E8_27-16	DDA Vertical Accumulator Initial Value 1. Value = [height (in lines) of the output window after scaling] -1. This is shown as H1 in Figure 9-2. This is used when MM81E8_28 = 1 and the secondary stream comes from secondary buffer 1.
MM81E8_15	Secondary Stream Vertical Interpolation Enable 0 = Vertical interpolation disabled 1 = Vertical interpolation enabled
MM81E8_28	Two DDA Vertical Accumulator Values Enable 0 = Use bits 11-0 for the DDA vertical accumulator value 1 = Use bits 11-0 when reading from buffer 0 and bits 27-16 when reading from buffer 1

9.3 KEYING/OUTPUT

A variety of output types can be composed from the streams described above. Keying is a way of selecting on a pixel by pixel basis which stream will be displayed. The keying modes are determined by MM8184_30-29 as follows:

Table 9-3. Streams Processor Keying Modes

MM8184 bits 30-29	Keying Mode	Description
00	Window	Rectangular secondary stream window overlaid on the primary stream. Blending requires that MM8184_31 = 1 (select secondary stream for keying) and opaque overlaying be disabled. The opaque overlay controls can only be used in this mode. Note that this mode will not work for the case where the user needs to pull down a graphics window over the video since the graphics window is defined as being under the video window.
01	Alpha	If 8184_31 = 0, this requires that CR67_7-4 = 0011b (KRGB 1.5.5.5) or 1101b (XRGB, X.8.8.8). K or X is the the alpha key. If MM8184_31 = 1, this requires that MM8190_26-24 = 011b or 111b.
10	Color	Use with an RGB stream. MM8184_31 can be either 0 or 1 (select either stream for keying).
11	Chroma	Used with a YUV or YCbCr stream. MM8184_31 must be set to 1 (select secondary stream for keying).

9.3.1 Opaque Rectangular Overlaying

This can be used only in Window Keying mode (MM8184_30-29 = 00b) and is enabled by setting MM81DC_31 to 1. The next step is to define when to stop fetching pixels for a line from memory and when to restart fetching them. The goal is to not fetch those pixels in the background window that are covered up by the opaque rectangular overlay window, thus saving memory bandwidth. Note that blending is not possible because the primary stream is not being fetched.

The first pixel that does not need to be fetched is at horizontal position X1 shown in Figure 9-2. This is programmed in MM8158_26-16. This must be converted into quadwords and then programmed in MM81DC_12-3. The value is (X1) x bytes per pixel/8. If the result is a fraction, it is rounded up to the next highest integer to ensure that the first pixel not fetched in inside the opaque overlay window.

Pixel fetching must start again before or at the last pixel position of the opaque overlay window. Using the terms in Figure 9-2, this position is X1 + W1, with W1 programmed in MM81FC_26-16. Converting to quadwords, the value is [X1 + W1] x bytes per pixel/8. If the result is a fraction, the result is truncated to the next lowest integer (minus 1) and programmed in MM81DC_28-19.

9.3.2 Blending

Blending can be used with any keying mode. The blender accepts the primary and secondary pixel streams and blends them with an arithmetic weighting. The result is then overlaid with the cursor and icon streams. Both blender inputs are RGB 8.8.8 from the outputs of the primary stream interpolator and secondary stream color space converter. Note that blending makes sense only when both streams are defined.

Blending uses two parameters. Ks (MM81A0_5-2 is the secondary stream blend coefficient. Kp (MM81A0_13-10) is the primary stream blend coefficient. When either the Ks or Kp value is reprogrammed, its new value does not take effect until the next VSYNC, so it can be programmed during frame display without disruptive effects. In all cases, Ks + Kp ≤ 8.

Blending to produce a dissolve effect is done according to the following formula:

[Pp x Kp + Ps x Ks]/8

Pp and Ps are the primary and secondary stream pixel colors respectively, both RGB 8.8.8. Kp and Ks are the primary and secondary stream weighting factors respectively. They are 4-bit values (max = 8). This weight values are applied to each of the three color values for the pixel.

If Kp = 8, Ks must = 0 and no blending occurs. As Ks is increased (and Kp decreased), the scene dissolves from primary stream to secondary stream.

If Ks = 0 and Kp is non-zero and decreasing, the effect is a fade according to the following:

Pp x {Kp/8]

9.3.3 Color Keying

Color keying is used when the stream source to be keyed is in RGB format (graphics). Both the primary and secondary streams support RGB formats.

A color key is defined by programming MM8184_23-0 with a specific RGB 8.8.8 color value. The number of bits to compare for each color is specified in MM8184_26-24. For 8-bpp modes, color keying is based on the 8-bit CLUT index, which is compared with bits 7-0 of MM8184. Bits 23-8 must be all 0's. For 15- and 16-bpp modes, low order 0's are added to form a 24-bit color key. If this value matches the value programmed in MM8184_23-0, the key is generated and blending is enabled. If there is no match, blending does not occur and the stream pixel used to generate the key (as selected by MM8184_31) is displayed.

9.3.4 Alpha Keying

Alpha keying is a special case of color keying. If the input format is KRGB-16 (1.5.5.5), the most significant bit of each pixel value is used as a color key. If this value matches the value programmed in MM8184_23-0, the key is generated and blending is enabled. If there is no match, the corresponding other stream pixel is displayed.

If the input format is XRGB-32 (X.8.8.8), the most significant byte of each pixel value is used as a color key. If this value matches the value programmed in MM8184_23-0, the key is generated and blending is enabled. If there is no match, the corresponding other stream pixel is displayed..

9.3.5 Chroma Keying

Chroma keying is used when the stream source is YUV or YCbCr (video). This is only possible for the secondary stream, so MM8184_31 must be set to 1.

The chroma key is specified as a range of color values. The lower bound value is defined in MM8184_23-0. The upper bound value is defined in MM8194_23-0. If the secondary stream pixel color

value falls within this range (inclusive of the lower and upper bounds), the Streams Processor displays the corresponding pixel from the primary stream. If the secondary stream pixel color is outside this range, the secondary stream pixel is displayed.

9.3.6 Color Adjustment

Color adjustment should be enabled only for YUV/YCbCr secondary stream formats. They must be disabled (MM819C_15 = 0 and MM819C_31 = 0) for secondary stream RGB formats.

MM819C - Color Adjustment Register

Bits 7-0 Brightness Control

Value = SBBBBBBB

where S is the sign bit (1 = negative) and BBBBBBB is the brightness adjustment factor. The larger the number, the greater the brightness. The programmed value is multiplied by 2 by the hardware. The value is in 2's complement format.

Bits 12-8 Contrast Control

Value = C.CCCC

Where C.CCCC is the contrast adjustment, which can vary from 0 to 1.9375. The value is in 2's complement format.

Bit 15 Brightness and Contrast Enable
0 = Brightness and contrast control disabled
1 = Brightness and contrast control enabled

Bit 20-16 Hue and Saturation Factor 1

Value = SF.FFF

where S is the sign bit (1 = negative) and the F.FFF is the factor [SAT * cos A]. SAT is the saturation, which can vary from -2 to 1.875 and A is the hue angle, the cosine of which varies from -1 to +1. The value is in 2's complement format.

9.3.7 Window Location

The starting X,Y coordinates and window size for the primary stream are specified by programming standard CRT control registers. The starting X,Y coordinates and window size for the secondary stream are specified in MM81F8 and MM81FC respectively.

9.4 STREAMS FIFO CONTROL

Several register control streams FIFO performance. These are listed in Table 9-4.

Table 9-4. Streams FIFO Control Registers

Register	Description
CR7B	Primary Stream 1 Timeout (Controller 1 is source)
CR7C	Primary Stream 2 Timeout (Controller 2 is source)
CR7D	Secondary Stream Timeout
CR85	Primary Stream 1 Threshold (Controller 1 is source)
CR86	Primary Stream 2 Threshold (Controller 2 is source)
CR87	Secondary Stream Threshold

Section 10: CRT and TV Interfaces

This section describes the CRT and TV hardware interface, generation of the respective outputs, and various issues related to the DACs used to generate these outputs.

10.1 CRT INTERFACE

The CRT hardware interface consists of analog RGB signals, horizontal and vertical syncs and, optionally, DDC communications. The latter is discussed in Section 13.4.

CRT analog RGB output (AR, AG, AB) is generated by three internal 8-bit DACs. For 8 bits/pixel CRT modes, the DACs are fed by one of two internal color look-up table (CLUT) RAMs. See Section 10.3 below for a description of how each CLUT is assigned to a DAC. Each CLUT provides 256 6-bit words for each color. A 24-bit CLUT bypass is provided for 15/16- and 24-bit color modes. Figure 10-1 shows the internal block diagram for the DACs and one of the CLUTs.

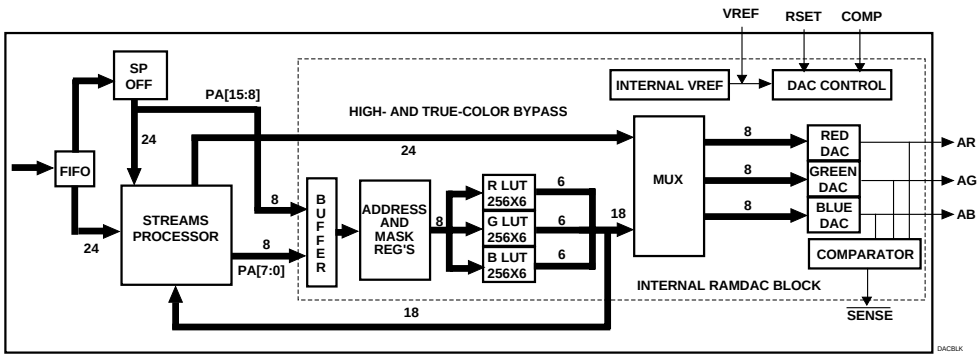


Figure 10-1. Internal RAMDAC Block Diagram

Table 10-1. ViRGE/MX Color Modes

CR67 Bits 7-4	PA Bits	Description
0000	7:0	4- or 8-bit color (CLUT) - Default
0011	15:0	15-bit color (CLUT Bypass)
0101	15:0	16-bit color (CLUT Bypass)
0111	23:0	24-bit packed (CLUT Bypass)
1101	23:0	24-bit unpacked color (X888) (CLUT Bypass)

10.1.1 Operating Modes

With the Streams Processor off (CR67_2 = 0), the secondary stream is disabled. The primary stream is processed by the selected controller. With the Streams Processor on (CR67_2 = 1), the secondary stream is enabled.

10.1.2 Color Modes

The ViRGE/MX internal DAC provides 5 color modes of the following 2 primary types:

1. 8 bits (low byte of the internal pixel address bus) are latched each pixel clock and are used to select a CLUT location.
2. 15 or 16 bits (lower two bytes of the internal pixel address bus) or 24 bits (all three bytes of the internal address bus) are transferred directly to the DACs each pixel clock.

Each of the 5 color modes is listed in Table 10-1. The desired mode is selected by programming bits 7-4 of CR67.

10.1.2.1 4 or 8 Bits/Pixel

This mode is selected by setting bits 7-4 of CR67 to 0000b. In this mode, the low 8 internal pixel address bus bits are ANDed with the contents of the Pixel Read Mask register (3C6H). The result of the AND operation selects one of 256 CLUT locations. This results in the output of 6 bits of color information to each of the DACs.

10.1.2.2 15/16-Bits/Pixel

These modes are selected by setting bits 7-4 of CR67 to 0011b (15 bits/pixel) or 0101b (16 bits/pixel). In either case, one pixel is transferred to the DAC each VCLK cycle via the CLUT bypass.

10.1.2.3 Packed 24 Bits/Pixel

This mode is selected by setting bits 7-4 of CR67 to 0111b. Each pixel is stored in 24 bits of memory. One pixel is transferred to the DACs each VCLK cycle via the CLUT bypass.

10.1.2.4 Unpacked 24 Bits/Pixel

This mode is selected by setting bits 7-4 of CR67 to 1101b. Each pixel is stored in 32 bits of memory. One pixel is transferred to the DACs each VCLK cycle via the CLUT bypass.

10.1.3 CRT DAC SENSE Generation

The internal CRT DAC contains analog voltage comparators. These drive the internal $\overline{\text{SENSE}}$ signal active low whenever the output on any of the AR, AG or AB pins exceeds 330 mV ± 20%. The state of this internal signal can be read via bit 4 of 3C2H. This information can be used to detect the existence and type of monitor (color/mono) connected to the system.

10.1.4 BLANK Pedestal

$\overline{\text{BLANK}}$ pedestal support is enabled by setting SR27_3 to 1. This white level output remains at 17.6 mA (typical) above the black level output. However, the black level output is raised to 1.45 mA (typical) over the $\overline{\text{BLANK}}$ output level of 0 mA. RAMDAC output using the $\overline{\text{BLANK}}$ pedestal is recommended for some monitors.

10.1.5 CRT DAC Signature Analysis

DAC signature analysis is a method of testing that the video data pipeline is operating correctly.

10.1.5.1 Signature Analysis Steps

1. Set up the desired mode and eliminate all borders ($\overline{\text{BLANK}}$ active during the entire non-active display period). To do this, set CR33_5 to 1. This does not quite work for the right border, so CR65_4-3 are used to delay $\overline{\text{BLANK}}$ by DCLK to produce the desired condition.
2. Wait until the VSYNC period. 3DAH_3 = 1 indicates active VSYNC. Alternately, set CR32_4 = 1 to enable interrupts. Set CR11_4 = 1 and CR11_5 = 0 to enable the VSYNC interrupt. Then poll for 3C2H_7 = 1. (The following two steps must take place during the blanking period. Using the VSYNC period is safe and this is easier to detect. The test could also be run between HSYNCs, but these are harder to detect.)
3. Reset the signature register by toggling SR18_1 from low to high to low.
4. Set SR18_0 to 1 to enable clocking of the signature register.
5. Generate a known and repeatable sequence of pixels to the DAC during the next non-blanking period. Each pixel is logically mixed with the current signature register contents and the result is left in the signature register.
6. Wait for the next VSYNC active, then clear SR18_0 to 0 to disable clocking of the signature register.
7. Toggle SR18_2 from low to high to low to read out red signature data, then read this data from CR6E.
8. Toggle SR18_3 from low to high to low to read out green signature data, then read this data from CR6E.
9. Toggle SR18_4 from low to high to low to read out blue signature data, then read this data from CR6E.

The expected result for a given test can be manually calculated from the logic equations used to update the signature register. These are given below. In addition, all tests using the same input data stream should produce the same result.

10.1.5.2 Signature Generation

A byte of data (IN) is read in logically and mixed with a byte of all 0's. The result (Q) is stored and then mixed with the next IN byte, resulting in a new Q value (Qnext). This process is repeated until all data is read in, at which time the final Q value is inverted. This is the signature that is read from the signature register.

Bits 0-6 of each Q value are generated by the following logic:

Qnext[k-1] = XNOR(IN[k], Q[K]), k = 1 to 7

Bit 7 of each Q value is generated by the following logic:

Qnext[7] = XNOR(XNOR(IN[0], Q[0]), XNOR(IN[3], Q[3]))

Signature output = NOT Q (for the final Q byte)

10.2 TV INTERFACE

ViRGE/MX provides a flicker filter and encoder for NTSC/PAL output to a television. TV output can be done concurrently with CRT and flat panel output. See Section 11.4 for a description of how this is done. Flicker filter data can optionally be output to the CRT DAC for support of an external encoder.

10.2.1 Flicker Filtering

Flicker filtering improves the quality of graphics data displayed on a TV. The flicker filter function takes non-interlaced 24-bit graphics (RGB) data from a graphics controller or the Streams Processor and converts it into interlaced YCbCr data to be used by the TV encoder. Because of the conversion from non-interlaced to interlaced format, data is clocked into the flicker filter at DCLK and clocked out of the flicker filter to the encoder at DCLK/2.

Flicker filtering is not required for motion video. Secondary stream data is often motion video, so SR70_5 provides the option of disabling flicker filtering for the secondary stream.

Flicker filtering is enabled by setting SR70_0 to 1. The data source for input to the flicker filter is Controller 1 if SR30_2 = 0 and Controller 2 if SR30_2 = 1. Since the TV subcarrier frequency must be very accurate, use of the DCLK2 PLL may be required to drive the controller providing TV output because it has higher resolution than the DCLK1 PLL. For proper flicker filter operation, CR16 (vertical blank end) must be programmed with the same value as CR6 (8 LSBs of the vertical total).

For graphics modes, if the number of active video lines will be larger than can be displayed by the TV monitor, overscan compensation (underscanning) must be used. This is performed by the graphics controller before sending the data to the flicker filter. Underscanning is never used in text modes.

Underscanning is vertical decimation. SR7E is programmed to enable underscanning, define the starting line and the interval between line deletions. The number of lines deleted per frame is programmed in SR7F. The method (different or same lines in odd/even field) is determined via SR7D_0.

SR74_2 enables underscanning for the hardware cursor. SR74_3 enables underscanning for the hardware icon. However, whether or not underscanning is enabled for the cursor and icon, their position on the screen is not automatically adjusted for deleted lines. This must be done via software. Further, underscanning cannot be performed on a secondary stream. Consequently, it should only be used in a non-enhanced graphics mode with no hardware cursor or secondary stream, e.g., VGA mode 12. Another alternative is to use a special graphics mode for TV output. For example, since most monitors support at least 440 active lines, a 640x440 mode can be created that allows use of all functions (hardware cursor, hardware icon, secondary stream) without need of underscanning.

RGB data from the controller is converted to YCbCr format before filtering. SR70_2 selects between 4:2:2 (= 0) and 4:1:1 {= 1) formats. Use of the latter is required if the active horizontal area is larger than 720 pixels (2 bytes/pixel). This conversion normally uses chroma filtering (SR70_3 = 0, default). This can be disabled by setting SR70_3 to 1. SR80-SR88 provide control over the color space conversion by allowing specification of the conversion weights for each component. The CCIR 601 standards for each weight are provided in the appropriate register.

Flicker filtering combines two or three lines to form a single line. Two lines are combined if SR70_1 = 0. Three lines are used if SR70_1 = 1. If the latter case is selected, secondary stream vertical interpolation cannot also be enabled. SR72_0 = 0 selects filtering applied to all color components (Y, Cr, Cb). SR72_0 = 1 selects filtering applied only to the Y component.

The contribution of each input to the output is specified via the filtering fraction (SR71_2-0). This value applies whenever Set Interpolative Threshold (SIT) is not enabled (SR72_1 = 0) or when SIT is enabled (SR72_1 = 1) and the Y difference is greater than or equal to the SIT threshold value specified in SR73_7-0. If SIT is enabled and the Y difference is less than the SIT threshold value, no vertical filtering is done.

Aperture correction/inverse aperture correction provides a non-linear adjustment for the Y values. The user defines three Y value regions. Aperture correction essentially brightens Y's in the high region, dims values in the low region, and variably affects values in the mid region. This can, for example, improve the appearance of text. Inverse aperture correction produces the opposite effect (reduces the range of Y's). This may improve flicker filtered graphics. Aperture correction is based on the following registers:

SR74_7-0 - Aperture Correction Value (AC)
SR75_7-0 - Aperture Correction Low Threshold Value (ACL)
SR76_7-0 - Aperture Correction Mid Threshold Value (ACM)
SR77_7-0 - Aperture Correction High Threshold Value (ACH)

If SR72_3-2 = 01b, the aperture correction logic is based on the following algorithm:

If $Y \geq ACH$ then $Y_{OUT} = Y + AC$
else if $Y < ACH$ and $Y \geq ACM$ then $Y_{OUT} = Y - AC$
else if $Y < ACM$ and $Y \geq ACL$ then $Y_{OUT} = Y + AC$
else if $Y < ACL$ then $Y_{OUT} = Y - AC$.

If SR72_3-2 = 10b, inverse aperture correction logic is based on the following algorithm:

If $Y \geq ACH$ then Yout = Y - AC
else if $Y < ACH$ and $Y \geq ACM$ then Yout = Y + AC
else if $Y < ACM$ and $Y \geq ACL$ then Yout = Y - AC
else if $Y < ACL$ then Yout = Y + AC.

The flicker filter output to the TV encoder can be clipped. SR71_4 = 1 provides clipping for luminance (Y) data (from 0 to 255 to 0 to 219). If this is done, the Y offset can be set to 16 by setting SR71_5 to 1. SR71_6 = 1 provides chrominance (CbCr) clipping (from -128 to 127 to -112 to 112).

10.2.2 TV Encoding

ViRGE/MX explicitly supports 3 output formats (with variations): U.S. NTSC, Japanese NTSC and PAL. Bit 5 of CR3D selects between NTSC (= 0) and PAL (= 1) output. Bit 7 of CR3D selects between U.S. NTSC (= 0) and Japanese NTSC (=1). The specifications for these formats and their variations are provided by the CCIR 601 standard. Generation of the desired output requires specification of the following:

- TV VSYNC delay
- Subcarrier frequency adjustment
- U/V color burst amplitude
- Horizontal signal timings

As described above, the flicker filter takes non-interlaced RGB data at DCLK rate and outputs interlaced YCbCr data at DCLK/2 rate. This process also halves the HSYNC and puts it out of phase with VSYNC. SR78_7-0 is programmed to re-align the active edges of these two signals.

The subcarrier frequency must be very exact. SR7B and SR7C provide a way of adjusting the subcarrier frequency with respect to the DCLK frequency to achieve the required level of accuracy.

The U/V color burst amplitude and horizontal timings are defined by the CCIR 601 standard for each format. The appropriate values for the standard outputs are given in tables below. Programmability allows support for other variations.

The TV encoder drives the AY and AC (analog luminance and chromanance) outputs for a TV monitor. TV ouput is enabled by CR3D_0 = 1. The output types are controlled by CR3D_2-1 as shown in the following table:

Table 10-2. TV Output Options

CR3D bits 2-1	AY	AC	Notes
00	Luma	Chroma	S-Video
11	Comp	Comp	

A single S-Video output is available, with the luminance output on the AY pin and the chromanance output on the AC pin. Alternately, the single composite signal can be output on both AY and AC.

Bit 4 selects between color (= 0) and black and white (= 1) output.

10.2.3 TV DAC SENSE Generation

TV DAC $\overline{\text{SENSE}}$ generation is enabled by setting SR19_4 to 1. SR79 is programmed with a value. This value is driven to the DAC and converted to the AY output to be used by the $\overline{\text{SENSE}}$ circuit. Similarly, SR7A is programmed with a value. This value is driven to the DAC and converted to the AC output to

be used by the $\overline{\text{SENSE}}$ circuit. The Y and C sense results can be read from SR1B_1 and SR1B_1 respectively. CR3D_0 must be set to 1 to enable AY and AC output.

10.2.4 External Encoder Support

SR70_7 = 1 enables output to an external TV encoder. Data normally sent to the TV DAC from the flicker filter is instead routed to the CRT DAC. Y data is output on the AR pin, Cb (U) data is output on the AG pin and Cr (V) data is output on the AB pin. The chrominance outputs are converted to unsigned values. An external analog MUX is required on the AR, AG, AB lines to allow both TV and CRT operation to be supported. Alternately, SR30_7 = 1 enables output of flicker filter data to an external encoder via FPD[35:24].

10.3 CLUT and DAC ISSUES

There are two color look-up table RAMs (CLUT1 and CLUT2) and two DACs (CRT DAC and TV DAC). This section describes how they are paired and accessed. The issues of DAC snoop and signature analysis are also discussed.

10.3.1 CLUT/DAC Assignment

CLUT1 is assigned to the controller sourcing the Streams Processor. If SR30_1 = 0, Controller 1 sources the Streams processor and CLUT 1 is assigned to it. If SR30_1 = 1, Controller 2 is assigned to the Streams Processor and CLUT1 is assigned to it. CLUT2 is then assigned to controller not assigned to the Streams Processor. Note that this assignment is independent of enabling of the Streams Processor. The CRT DAC is assigned to one of the controllers via SR31_2 (0 = Controller 1, 1 = Controller 2). The TV DAC is assigned to one of the controllers via SR30_2 (0 = Controller 1, 1 = Controller 2).These combination determine which CLUT is assigned to the which DAC. Note that the same CLUT could be assigned to both DACs.

10.3.2 DAC Register Access

The standard VGA DAC register set (3C6H - 3C9H) is used to access the internal DAC registers and the two CLUTs. SR47_1-0 control the updating of the CLUTs. If SR47_1-0 = 00b, CLUT1 and CLUT2 are both enabled. A write will update both CLUTs identically (mirroring). Only CLUT1 is enabled for reading. If SR47_1-0 = 01b, only CLUT1 is enabled for reading and writing. If SR47_1-0 = 10b, only CLUT2 is enabled for reading and writing. Note that if an internal DAC register access is made, that access will be directed to the DAC or DACs associated with the CLUT enabled for access.

10.3.3 DAC Snooping

Setting bit 5 of the Command PCI configuration space register (Index 04H) to 1 causes ViRGE/MX to snoop for DAC writes. This means that ViRGE/MX will write the data to its local selected DAC but will not claim the cycle by asserting $\overline{\text{DEVSEL}}$. This allows the ISA controller to also generate a write cycle to a secondary DAC. ViRGE/MX always provides the data for DAC reads.

If bit 5 of the PCI Command register is cleared to 0, ViRGE/MX claims all DAC read and write cycles.

Section 11: Flat Panel Interface

ViRGE/MX supports a variety of color STN and TFT flat panels. Flat panel display is enabled by setting SR31_4 = 1. This section describes the control and data interfaces for each type. Operation of a flat panel in conjunction with a CRT is also described.

11.1 STN PANEL SUPPORT

STN panel support is selected when SR39_1-0 = 10b.

11.1.1 STN Panel Selection

ViRGE/MX supports either a single-scan (SS-STN) or a dual-scan (DD-STN) STN panel. The type is selected via SR30_0 as follows:

0 = DD-STN panel
1 = SS-STN panel

When DD-STN panel operation is selected, frame acceleration is automatically used in all modes of operation. This means the panel will be refreshed at twice the CRT rate. For example, if the flat panel timing registers are programmed for a refresh rate of 60 Hz, the actual refresh rate will be be 120 Hz.

SR3D_2-0 define the pixel data bus size as follows:

000 = 16-bit STN
001 = 8-bit STN
010 = 24-bit STN

Pixel data is output on some combination of the the FPD[35:0] pins, depending on the pixel data bus size and the setting of SR3D_3. This is shown in Tables 11-1 and 11-2.

11.1.2 STN Panel Timing

Functional timings for the data outputs of all the STN panel configurations listed in Tables 11-1 and 11-2 are given in Figures 11-1 through 11-6.

Table 11-1. STN Flat Panel Data Outputs (SR3D_3 = 0)

SR30_0	1	1	1	0	0	0
SR39_1-0	10	10	10	10	10	10
SR3D_2-0	001	000	010	010	000	010
Pin Name	**SS-STN 8**	**SS-STN 16**	**SS-STN 24**	**DD-STN 8**	**DD-STN 16**	**DD-STN 24**
FPD0	R0	R0	R0	LR0	LR0	LR0
FPD1	G0	G0	G0			LR3
FPD2	B0	B0	B0	LG0	LG0	LG0
FPD3	R1	R1	R1			
FPD4	G1	G1	G1	LB0	LB0	LB0
FPD5	B1	B1	B1			
FPD6	R2	R2	R2	LR1	LR1	LR1
FPD7	G2	G2	G2			LG3
FPD8		B2	B2		LG1	LG1
FPD9		R3	R3			
FPD10		G3	G3		LB1	LB1
FPD11		B3	B3			
FPD12		R4	R4		LR2	LR2
FPD13		G4	G4			LB3
FPD14		B4	B4		LG2	LG2
FPD15		R5	R5			
FPD16			G5			LB2
FPD17			B5			
FPD18			R6	UR0	UR0	UR0
FPD19			G6			UR3
FPD20			B6	UG0	UG0	UG0
FPD21			R7			
FPD22			G7	UB0	UB0	UB0
FPD23			B7			
FPD24				UR1	UR1	UR1
FPD25						UG3
FPD26					UG1	UG1
FPD27						
FPD28					UB1	UB1
FPD29						
FPD30					UR2	UR2
FPD31						UB3
FPD32					UG2	UG2
FPD33						
FPD34						UB2
FPD35						

Table 11-2. STN Flat Panel Data Outputs (SR3D_3 = 1)

SR30_0	0	0
SR39_1-0	10	10
SR3D_2-0	000	010
Pin Name	**DD-STN 16**	**DD-STN 24**
FPD0		LB3
FPD1		LB2
FPD2	LB1	LB1
FPD3	LB0	LB0
FPD4		UB3
FPD5		UB2
FPD6	UB1	UB1
FPD7	UB0	UB0
FPD8		LG3
FPD9	LG2	LG2
FPD10	LG1	LG1
FPD11	LG0	LG0
FPD12		UG3
FPD13	UG2	UG2
FPD14	UG1	UG1
FPD15	UG0	UG0
FPD16		LR3
FPD17	LR2	LR2
FPD18	LR1	LR1
FPD19	LR0	LR0
FPD20		UR3
FPD21	UR2	UR2
FPD22	UR1	UR1
FPD23	UR0	UR0
FPD24		
FPD25		
FPD26		
FPD27		
FPD28		
FPD29		
FPD30		
FPD31		
FPD32		
FPD33		
FPD34		
FPD35		

11.1.3 STN Panel Control

Selection of an STN panel configures several pins specifically for STN control.

The polarity of the flat panel data can be changed to active low by programming SR32_4 to 1. The drive strength of the panel data is specified via SR3D-6. The drive strength for the clock is specified via SR3D_7.

The modulation (MOD) signal is output on pin B15 for STN panels when SR34_7 = 1. The modulation period is defined by SR34_6-0. SR35_4 selects the MOD clock. If MOD is not enabled, B15 outputs the FPDE display enable signal. The polarity of FPDE can be changed to active low by programming SR32_5 to 1.

Pin C4 provides the LP signal. The polarity of LP can be changed to active low by programming SR32_6 to 1.

Several controls are provided for LP and FPSCLK during vertical blanking. FPSCLK is normally stopped during non-display time by setting SR40_5 to 1. When SR3D_4 = 0, LP will run during vertical blanking. Setting SR3D_4 to 1 disables LP during vertical blank. Setting SR33_6 to 1 adds an extra LP when LP is disabled during vertical blanking. If SR3D_4 = 0 and SR3D_5 = 1, FPSCLK is disabled during the first line of vertical blanking. If SR40_5 = 0, FPSCLK runs continuously. FPSCLK can be delayed via SR40_3-1. Its polarity can be inverted via SR32_3.

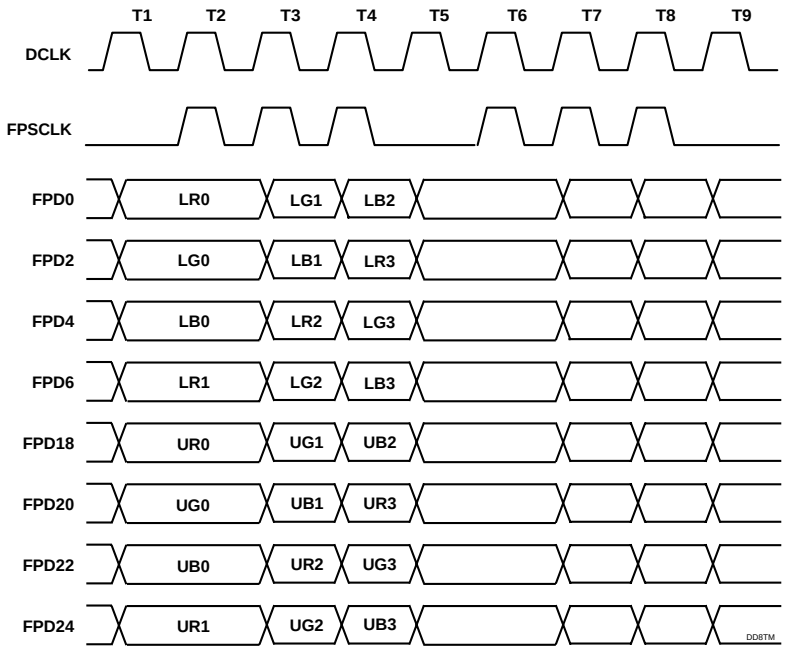


Figure 11-1. 8-bit Color DD-STN Panel Timing

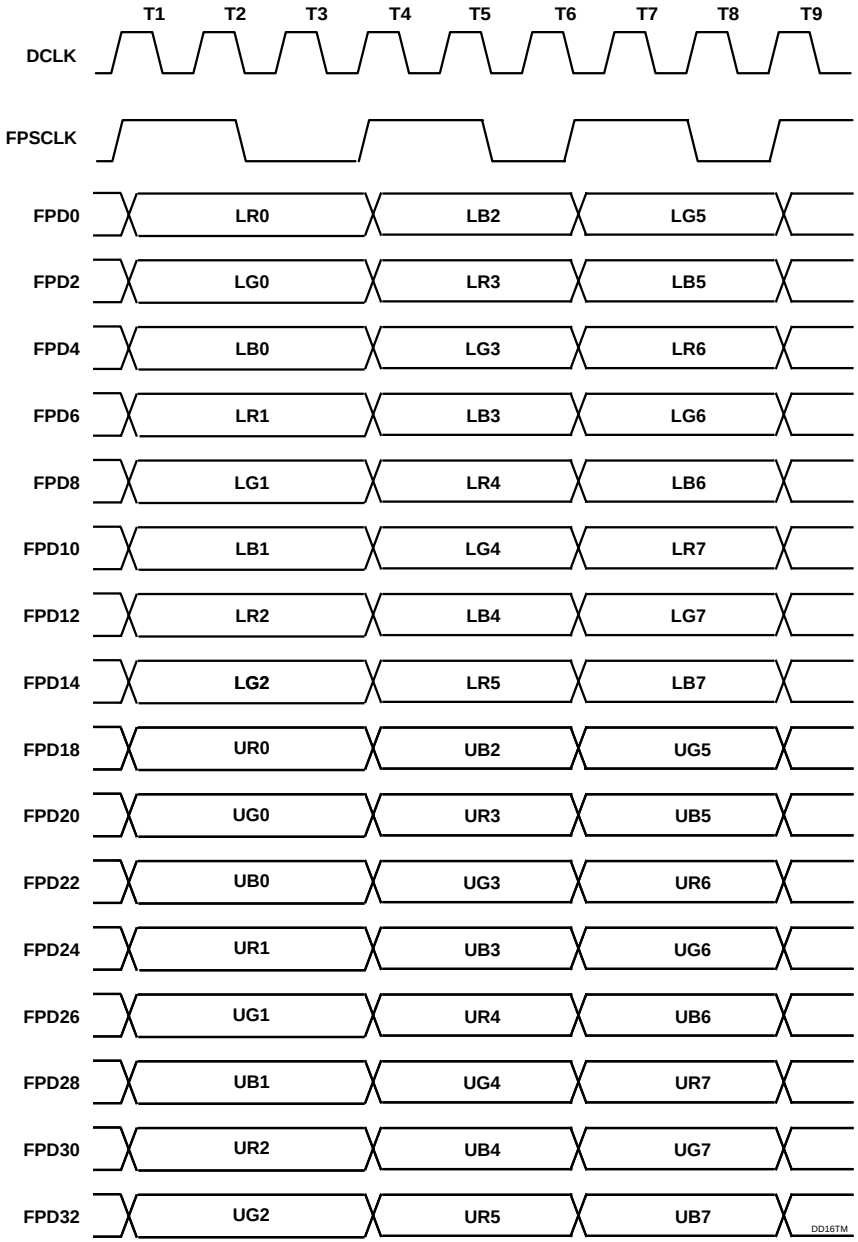


Figure 11-2. 16-bit Color DD-STN Panel Timing

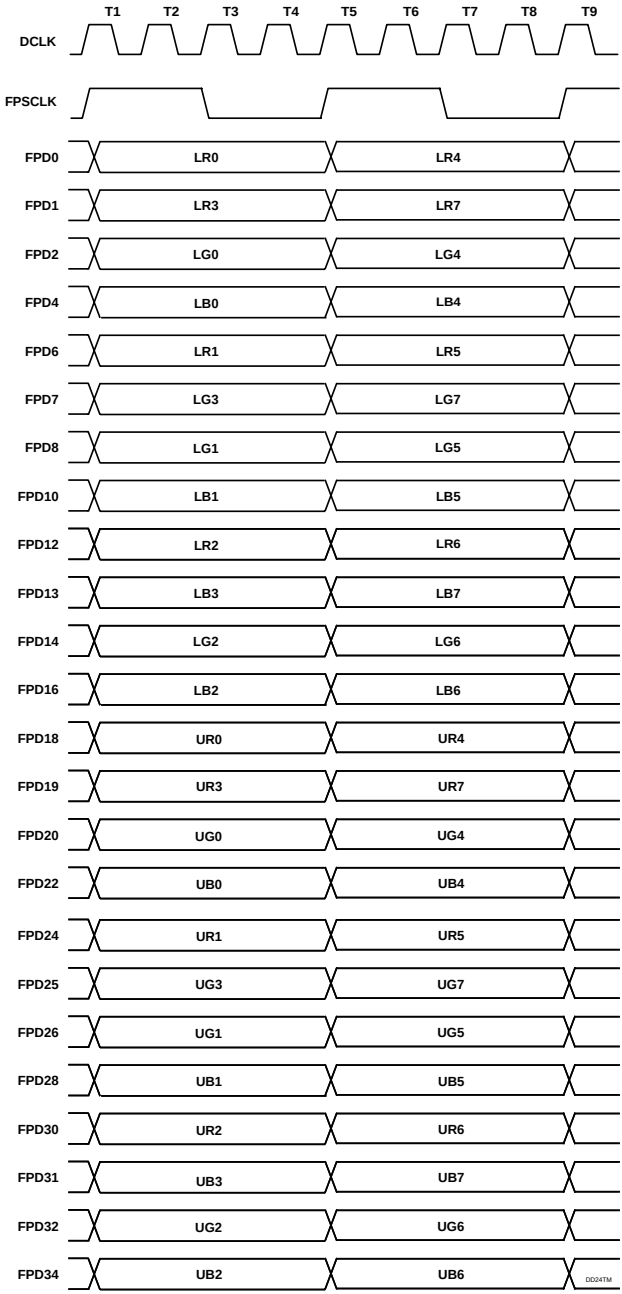


Figure 11-3. 24-bit Color DD-STN Panel Timing

Pin A3 provides the FLM (first line marker) signal. The polarity of FLM can be changed to active low by programming SR32_7 to 1.

Setting SR40_4 to 1 forces all flat panel data and control signals to logic 0.

11.1.4 STN Frame Rate Control

Frame rate control (FRC) for STN panels is used to display more grayscale levels than would normally be possible based on the 1 bit/color input. Each color bit is turned on or off over a series of frames to simulate intermediate colors.

Frame rate control is enabled automatically for STN panels. The number of frames over which bits are turned on or off to generate a single color determines the number of grayscale levels and is programmed in SR39_4-3 as follows:

00= 16 levels
01 = 8 levels
10 = Reserved
11 = Reserved

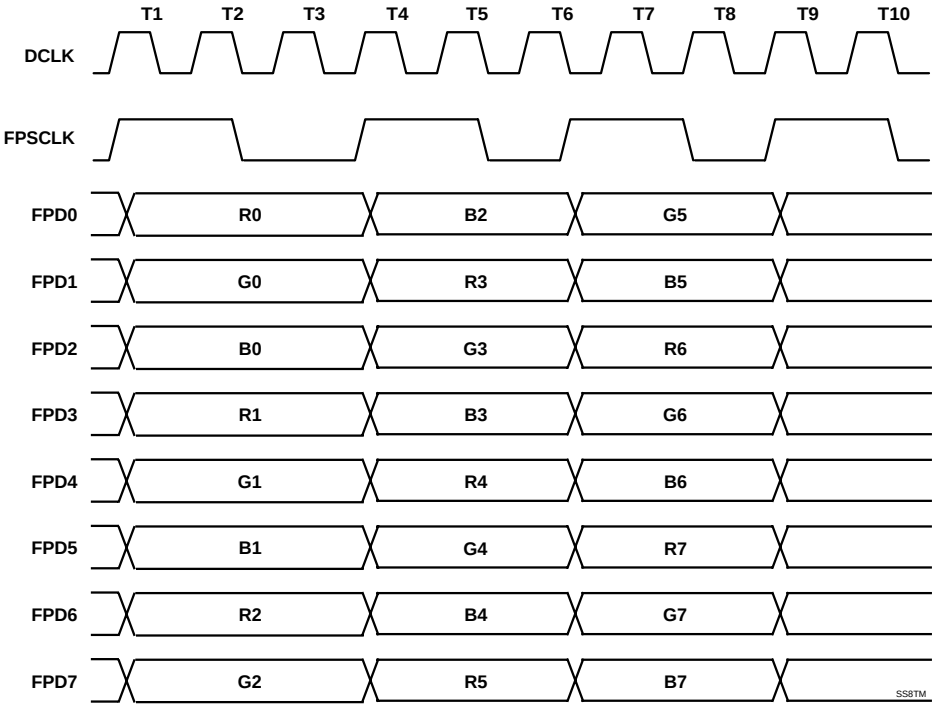


Figure 11-4. 8-bit Color SS-STN Panel Timing

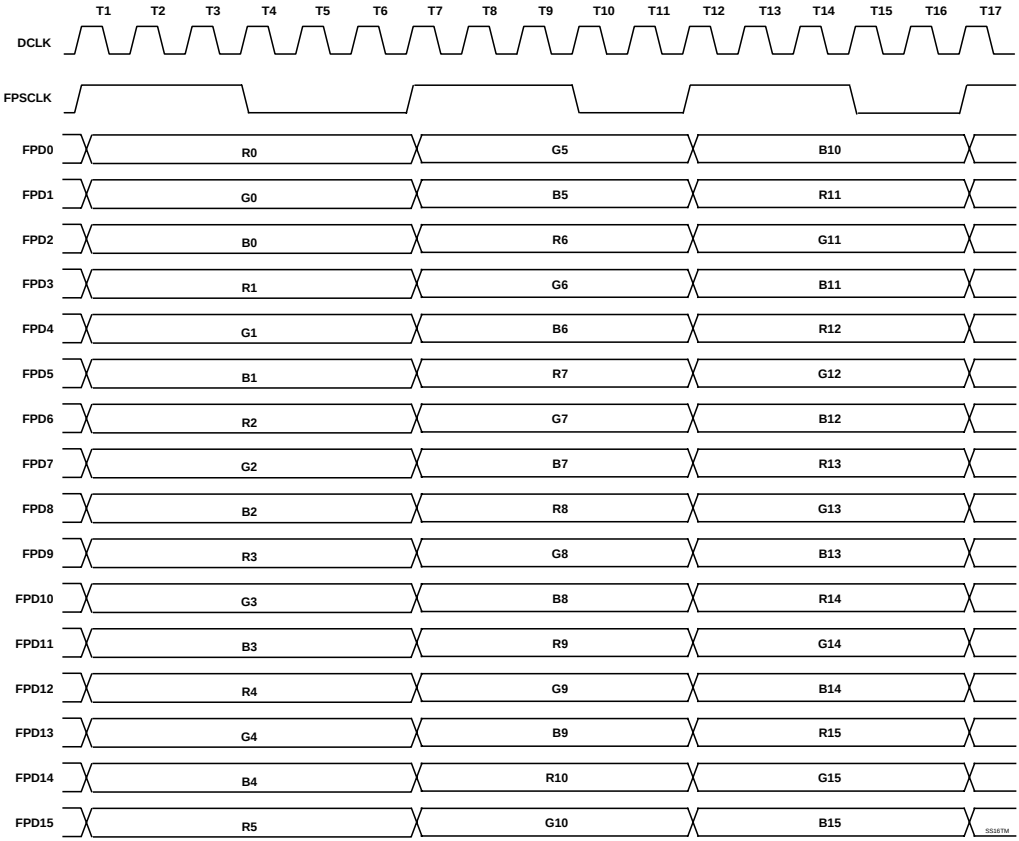


Figure 11-5. 16-bit Color SS-STN Panel Timing

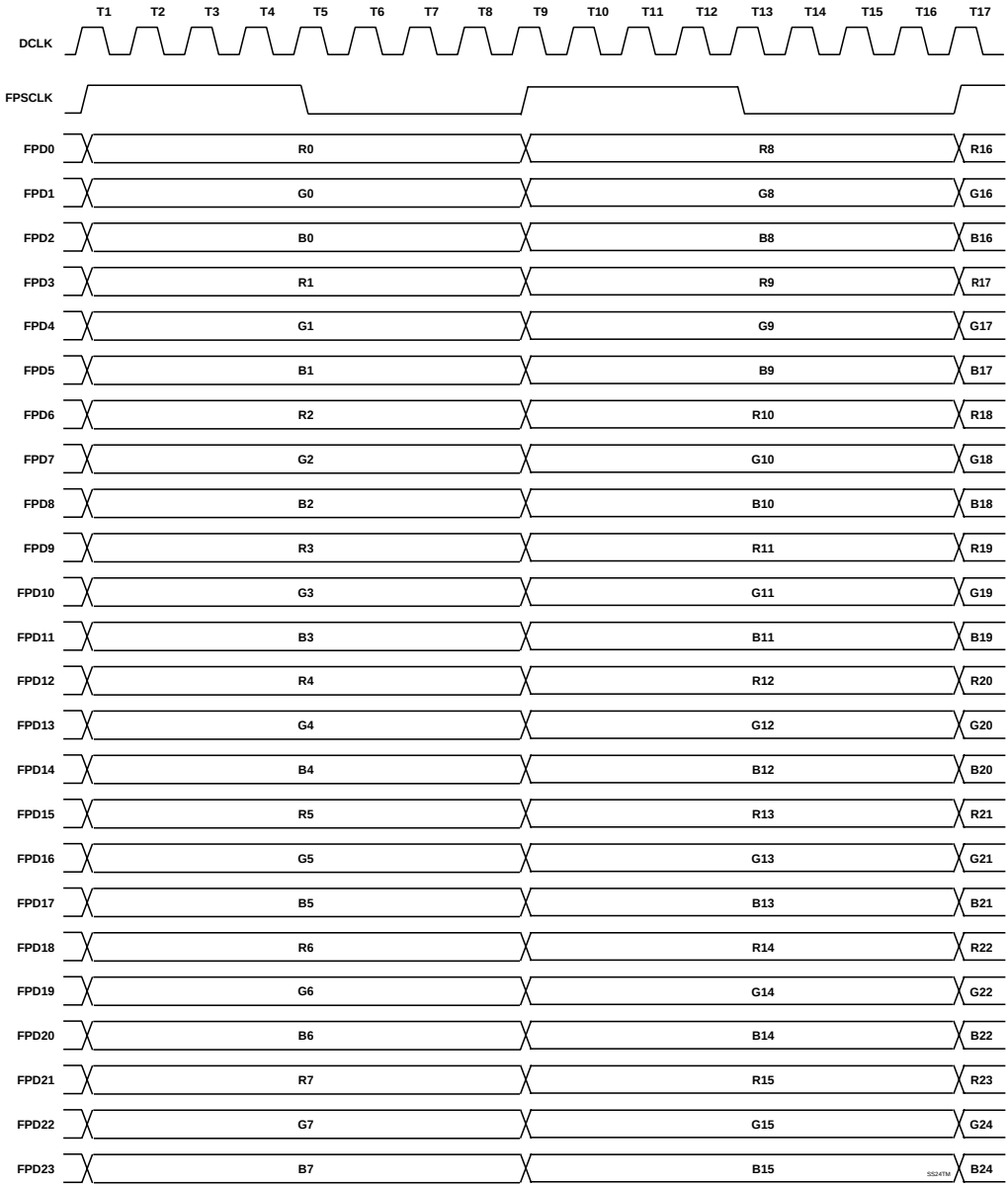


Figure 11-6. 24-bit Color SS-STN Panel Timing

If SR33_4 =1, 8 frame FRC is forced when secondary stream data is being output to the STN panel.

FRC weighting values are programmed via SR37 and SR38. SR3A and SR3B are used to tune the frame rate control for optimum quality. The algorithms and techniques used are proprietary.

11.1.5 STN Panel Dithering

Dithering is used to increase the apparent number of colors displayed. This is enabled by setting SR36_7-6 as follows:

00 = Dithering disabled
01 = Dither in all modes
10 = Dither in graphics modes only (no text)
11 = Dither in graphics modes with 8 bpp or more

The base color is selected by programming SR36_5-3 as follows:

000 = 8 bits (no dithering)
011 = 3 bits (8-level FRC)
100 = 4 bits (16-level FRC)

SR36_0 selects the number of bits of the 8-bit color value to use for dithering as follows:

0 = 2 bits (2x2 dither pattern)
1 = 4 bits (4x4 dither pattern)

11.1.6 Dual-Scan STN Frame Buffer

DD-STN panel operation requires off-screen video memory. The amount of memory is programmed in SR50 and SR51. The starting location of the DD-STN memory is specified in SR4F. These values are all programmed by the video BIOS at reset.

11.2 TFT PANEL SUPPORT

TFT panel support is selected when SR39_1-0 = 00b.

11.2.1 TFT Panel Selection

SR3D_2-0 define the pixel data bus size as follows:

000 = 1 pixel/clock TFT (9-, 12-, 15-, 18-bit)
001 = 1 pixel/clock TFT (24-bit)
010 = 2 pixels/clock TFT (2x9-, 2x12-, 2x18-bit)

The 2 pixels per clock modes halve the clock rate and clock two pixels on the falling edge of FPSCLK, thereby lowering EMI levels. SR40_6 is set to 1 to support this mode of operation.

Pixel data is output on some combination of the FPD[35:0] pins. The data outputs are shown in Table 11-3 AND 11-4, depending on the setting of SR3D_3.

11.2.2 TFT Panel Timing

TFT panel timing is very similar to CRT timing, with the FPDE signal functionally equivalent to the CRT $\overline{\text{BLANK}}$ signal (inverted). Functional timing for an 24-bit TFT panel clocked at one pixel per FPSCLK and a 36-bit (2x18) panel clocked at 2 pixels/FPSCLK are shown in Figure 11-7. Timings are the same for all types of TFT panels clocked at 1 pixel/FPSCLK, as is the case for all types of TFT panels clocked at 2 pixels/FPSCLK.

11.2.3 TFT Panel Control

Selection of a TFT panel configures several pins specifically for TFT control. The drive strengths of the panel clock and data are specified via SR3D_7-6.

The polarity of the flat panel data can be changed to active low by programming SR32_4 to 1.

Pin B15 becomes the FPDE display enable signal. The polarity of this signal can be changed to active low by setting SR32_5 to 1.

Pin C4 becomes the FPHSYNC signal. The polarity of this signal can be changed to active low by setting SR32_6 to 1.

Pin A3 becomes the FPVSYNC signal. The polarity of this signal can be changed to active low by setting SR32_7 to 1.

Pin C15 is the FPPOL polarity indicator signal for those panels that support it. It is available when SR40_7 = 1 and CR6F_0 = 1. FPPOL is supported for 18- and 24-bit 1 pixel/clock modes and for 2x18-bit 2 pixels/clock mode. Timing for this signal is shown in Figure 11-7.

SR40_5 allows FPSCLK to be enabled (=0) or disabled (=1) during non-display time. FPSCLK can be delayed via SR40_3-1.

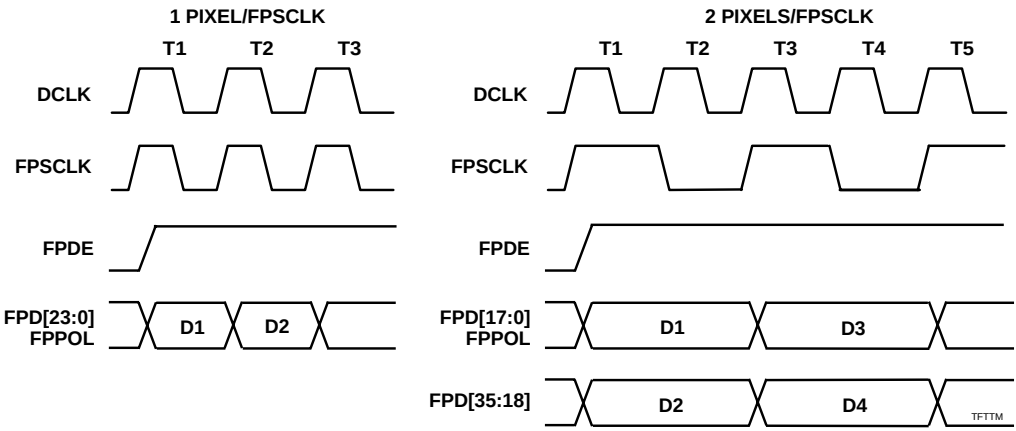


Figure 11-7. TFT Panel Timing

Table 11-3. TFT Flat Panel Data Outputs (SR3D_3 = 0)

SR30_0	1	1	1	1	1	1	1	1	1
SR36_5-3	011	011	100	100	101	101	110	110	000
SR39_1-0	00	00	00	00	00	00	00	00	00
SR3D_2-0	000	010	000	010	000	010	000	010	001
Pin Name	**TFT 9**	**TFT 2x9**	**TFT 12**	**TFT 2x12**	**TFT 15**	**TFT 2x15**	**TFT 18**	**TFT 2x18**	**TFT 24**
FPD0							R0	R00	R2
FPD1								R10	R0
FPD2					R0	R00	R1	R01	R3
FPD3						R10		R11	
FPD4			R0	R00	R1	R01	R2	R02	R4
FPD5				R10		R11		R12	
FPD6	R0	R00	R1	R01	R2	R02	R3	R03	R5
FPD7		R10		R11		R12		R13	R1
FPD8	R1	R01	R2	R02	R3	R03	R4	R04	R6
FPD9		R11		R12		R13		R14	
FPD10	R2	R02	R3	R03	R4	R04	R5	R05	R7
FPD11		R12		R13		R14		R15	
FPD12							G0	G00	G2
FPD13								G10	G0
FPD14					G0	G00	G1	G01	G3
FPD15						G10		G11	
FPD16			G0	G00	G1	G01	G2	G02	G4
FPD17				G10		G11		G12	
FPD18	G0	G00	G1	G01	G2	G02	G3	G03	G5
FPD19		G10		G11		G12		G13	G1
FPD20	G1	G01	G2	G02	G3	G03	G4	G04	G6
FPD21		G11		G12		G13		G14	
FPD22	G2	G02	G3	G03	G4	G04	G5	G05	G7
FPD23		G12		G13		G14		G15	
FPD24							B0	B00	B2
FPD25								B10	B0
FPD26					B0	B00	B1	B01	B3
FPD27						B10		B11	
FPD28			B0	B00	B1	B01	B2	B02	B4
FPD29				B10		B11		B12	
FPD30	B0	B00	B1	B01	B2	B02	B3	B03	B5
FPD31		B10		B11		B12		B13	B1
FPD32	B1	B01	B2	B02	B3	B03	B4	B04	B6
FPD33		B11		B12		B13		B14	
FPD34	B2	B02	B3	B03	B4	B04	B5	B05	B7
FPD35		B12		B13		B14		B15	

Table 11-4. TFT Flat Panel Data Outputs (SR3D_3 = 1)

SR30_0	1	1	1
SR36_5-3	110	110	000
SR39_1-0	00	00	00
SR3D_2-0	000	010	001
Pin Name	**TFT 18**	**TFT 2x18**	**TFT 24**
FPD0		R14	B0
FPD1		R15	B1
FPD2	B0	B00	B2
FPD3	B1	B01	B3
FPD4	B2	B02	B4
FPD5	B3	B03	B5
FPD6	B4	B04	B6
FPD7	B5	B05	B7
FPD8		R12	G0
FPD9		R13	G1
FPD10	G0	G00	G2
FPD11	G1	G01	G3
FPD12	G2	G02	G4
FPD13	G3	G03	G5
FPD14	G4	G04	G6
FPD15	G5	G05	G7
FPD16		R10	R0
FPD17		R11	R1
FPD18	R0	R00	R2
FPD19	R1	R01	R3
FPD20	R2	R02	R4
FPD21	R3	R03	R5
FPD22	R4	R04	R6
FPD23	R5	R05	R7
FPD24		G10	
FPD25		G11	
FPD26		G12	
FPD27		G13	
FPD28		G14	
FPD29		G15	
FPD30		B10	
FPD31		B11	
FPD32		B12	
FPD33		B13	
FPD34		B14	
FPD35		B15	

11.2.4 TFT Panel Dithering

As with STN panels, dithering is used to increase the apparent number of colors displayed. This is enabled by setting SR36_7-6 appropriately as follows:

00 = dithering disabled
01 = dithering enabled in all modes
10 = dither in graphics (not text) modes
11 = dither in graphics modes with 8bpp or more color

SR36_0 selects the dither pattern as follows:

0 = 2x2 pattern
1 = 4x4 pattern

The base color is selected by programming SR36_5-3 as follows:

000 = 8 bits (no dithering - 24-bit TFT
011 = 3 bits (9-bit TFT)
100 = 4 bits (12-bit TFT)
110 = 6 bits (18-bit TFT)

Note that all other values are illegal.

11.3 FLAT PANEL DISPLAY ENHANCEMENTS

ViRGE/MX features automatic centering for display modes that are smaller than the panel size. Additionally, horizontal and vertical expansion for both graphics and text modes enables low resolution modes to fill the available display area. Automatic centering and expansion is available only for Controller 1 and applies only to the primary stream. Software centering and expansion must be used for the secondary stream.

11.3.1 Automatic Centering

Automatic horizontal centering is enabled via SR54_4. Automatic vertical centering is enabled via SR56_4.

11.3.2 Horizontal Expansion

SR54_1-0 enable horizontal expansion for text modes. SR55_1-0 specify which text modes get expanded. SR54_3-2 enable horizontal expansion for graphics modes. SR55_4-2 specify which graphics modes get expanded. SR54_4 enables horizontal centering. SR54_6-5 = 1 enables horizontal expansion filtering. For horizontal expansion in VGA mode 13, SR62 must be programmed larger than SR61.

11.3.3 Vertical Expansion

SR56_1-0 enable vertical expansion for text modes. SR57_1-0 specify which text modes get expanded. SR56_3-2 enable vertical expansion for graphics modes. SR57_6-2 specify which graphics modes get expanded. SR56_4 enables vertical centering.

11.3.4 Pulse Width Modulation

Two pulse width modulation (PWM) signals are available to control panel brightness or contrast. SR52_0 = 1 enables PWM0. SR52_1 specifies the PWM0 clock source. SR52_6-4 specify the clock divide used to determine the final PWM0 pulse width (period). The duty cycle of the PWM1 pulse is controlled via SR53. SR52_7 = 1 enables PWM1. SR52_1 specifies the PWM1 clock source. SR52_6-4 specify the clock divide used to determine the final PWM1 pulse width (period). The duty cycle of the PWM1 pulse is controlled via SR3E.

PWM[1:0] active timing is coordinated with panel power sequencing. This is shown in Figure 11-8.

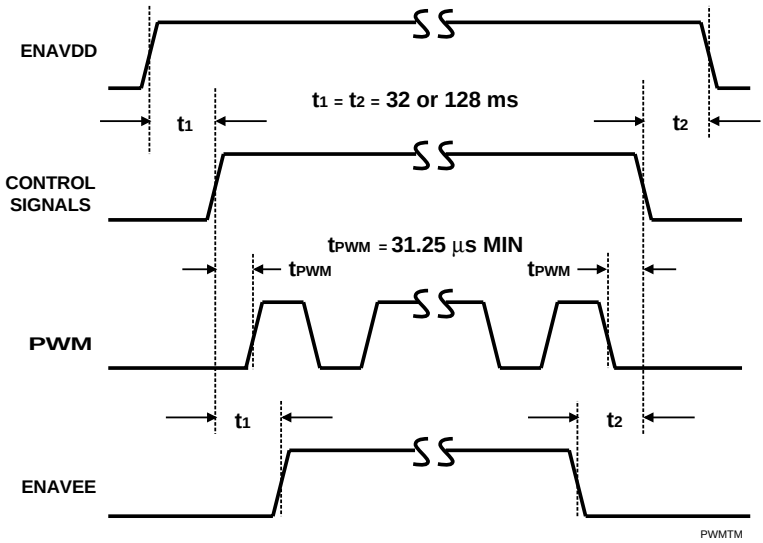


Figure 11-8. PWM Timing

11.3.5 Blinking

Character blinking can be set via CR43_3 to every 32 (= 0) or 64 (=1) frames. Cursor blinking can be set via CR43_6-5 as follows:

00 = blink every 16 frames
01 = blink every 32 frames
10 = blink every 64 frames

11.4 DuoView DISPLAY

ViRGE/MX has two CRT controllers (Controller 1 and Controller 2). It also has two DCLK PLLs, generating DCLK1 and DCLK2. Either DCLK can drive either controller, or the same DCLK can drive both controllers. Either controller can be used to drive a CRT and either can be used to drive a flat panel, or one controller can drive both. The Streams Processor can be used in conjunction with either controller, but not both. The major restriction is that controller 2 can only be used to display Enhanced modes (not VGA) and does not provide automatic flat panel expansion and centering.

This flexibility provides the ability to display one image on the CRT and a completely different image on the flat panel, each using different CRT timings. (TV can also be displayed - see section 10.) This section explains how to take advantage of this.

11.4.1 DuoView Display Setup

Flat panel controller usage is defined by SR31_1 as follows:

0 = Flat panel source is controller 1
1 = Flat panel source is controller 2 (no VGA)

The controller used by the CRT is defined by SR31_2 as follows:

0 = CRT source is controller 1
1 = CRT source is controller 2 (no VGA)

The Streams Processor source is defined by SR30_1 as follows:

0 = Controller 1 is Streams Processor source
1 = Controller 2 is Streams Processor source

The Controller 1 dot clock is defined by SR30_3 as follows:

0 = DCLK1 is Controller 1 dot clock
1 = DCLK2 is Controller 1 dot clock

The Controller 2 dot clock is defined by SR30_4 as follows:

0 = DCLK2 is Controller 2 dot clock
1 = DCLK1 is Controller 2 dot clock

Note that by default, DCLK1 drives Controller 1 and DCLK2 drives Controller 2.

Each controller has an associated color look-up table (CLUT). By default, CLUT1 and CLUT2 will be enabled and mirrored for CPU writes. The hardware cursor and hardware icon, if enabled, are shared by both controllers. By default, they are controlled by Controller 1.

The controller choices are based on the following considerations.

Flat Panel or CRT Only

Use Controller 1.

Simultaneous Display

Use Controller 1 for both CRT and flat panel.

This is a variation of DuoView where the CRT and flat panel images are displayed with almost identical timings. Normally, the flat panel timings are compromised for CRT VESA timings. Video output using the Streams Processor is displayed on both screens, as are the hardware cursor and/or hardware icon, if enabled. When this mode is used, TV can also be output with independent timings using the other controller and DCLK PLL.

DuoView Display

For this case, the CRT, TV or flat panel uses one controller and one of the remaining two displays uses the other. The choice depends on the need to display standard VGA modes or the need to have automatic expansion/centering, both of which require Controller 1. Note that only one screen can display video in this mode.

In DuoView mode, the hardware cursor can be displayed on either screen. SR31_7 = 0 selects cursor control by Controller 1 and SR31_7 = 1 selects cursor control by Controller 2. The hardware icon can also be displayed on either screen. SR31_6 = 0 selects icon control by Controller 1 and SR31_6 = 1 selects icon control by Controller 2.

In DuoView, if a text mode is used for one display, a text mode must also be used for the other display. The same is true for graphics modes. In other words, text and graphics modes cannot be mixed. If the same image is to be displayed on both the display devices but with different timings, both controllers must be used and VGA modes are not available.

11.4.2 DuoView Programming

ViRGE/MX has a large number of paired registers for control of timings and resolutions for CRT display. For example, there are two Horizontal Total (CR0) registers, one associated with CRT Controller 1 and the other with CRT Controller 2. Both have the same address, and control of read/write access to these registers is provided by a number of bits in SR26. SR26_3 controls write access to the CRT Controller 1 registers. A value of 0 (default) enables writes. SR26_2 controls write access to the CRT Controller 2 registers. A value of 0 (default) disables write access. Using these controls, a single write can update either of the paired registers or both.

Bit 0 and 1 of SR26 control read access of the paired registers.

The following registers (or register bits) are paired:

CR0-CR6; CR7-3-0, CR7_7-5, 3-0; CR8_6-5; CR9_7,5; CRC; CRD; CR10; CR11_7, 3-0; CR13, CR15-CR16; CR17_7, 2; CR33_0, CR33_2, CR33_3, CR33_5; CR33_7, CR35_5-4; CR3B; CR3C; CR42_5; CR51_5-4; CR5D; CR5E; CR63_4-0; CR65_4-3; CR67_7-4; CR69_4-0; CR71_5,1, CR90, CR91

Paired registers and bits are noted in the register descriptions.

A separate set of CRT timing registers is provided for flat panel operation. These are SR60 - SR6F, except SR67 is reserved. The values to be programmed in these registers are fixed for a given panel (not mode dependent as with a CRT). Therefore, they should be programmed only at reset. These registers are used by Controller 1 if SR31_1 = 0 and by Controller 2 if SR31_1 = 1.

Section 12: Local Peripheral Bus

The Local Peripheral Bus (LPB) is enabled when bit 0 of MMFF00 is set to 1. The LPB function provides the following:

- S3 Scenic Highway bidirectional interface interface to the Scenic/MX2 MPEG Audio/Video Decoder (glueless, bi-directional)
- Scenic Highway 8-bit or 16-bit interface to industry standard video digitizers
- Host Video Data Pass-through. This allows decimation of 32-bit CPU data being written to the frame buffer.
- VBI support
- 4-bit General Input Port and 4-bit General Output Port
- ZV- Port

The hardware interfaces are clocked by LCLK. This requires that MMFF00_24 be set to 1. Pass-through operation is clocked by SCLK by clearing MMFF00_24 to 0.

The internal block diagram for the LPB is shown in Figure 12-1.

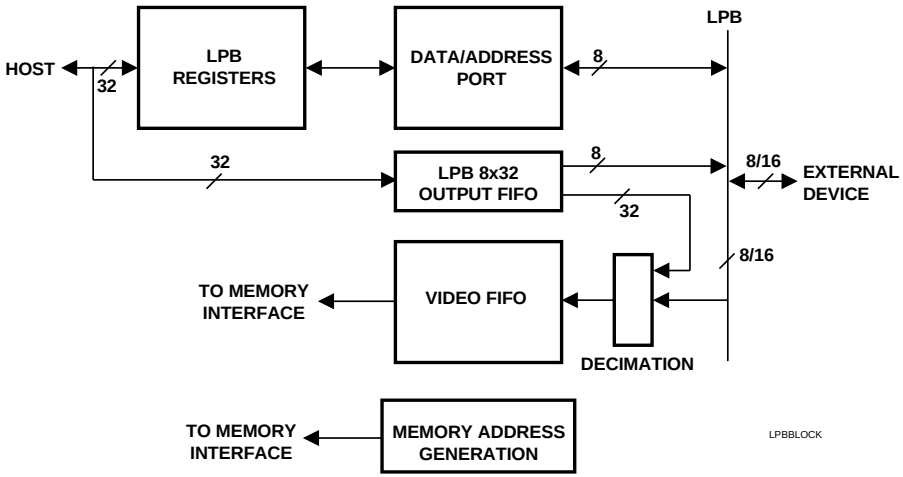


Figure 12-1. LPB Internal Block Diagram

12.1 BIDIRECTIONAL INTERFACE

The bidirectional interface is selected by setting MMFF00_3-1 to 000b. It provides a glueless interface to devices designed to use its protocol (such as the S3 Scenic/MX2). Use of this interface and the complete protocol are described in the LPB Specification available from S3.

12.2 DIGITIZER INTERFACE

ViRGE/MX provides a glueless interface to the industry-standard digitizers in Video 16 mode (MMFF00_3-1 = 001b) as shown in Figure 12-2. This section describes the interface to the Philips SAA7110 digitizer.

12.2.1 I^2C Interface for SAA7110

SAA7110 registers are programmed via a serial I^2C interface. This interface is described in Section 13.

12.2.2 SAA7110 Video Input

The following setup is done for SAA7110 video input:

- ViRGE/MX is placed in Video 16 mode (MMFF00_3-1 = 001b)
- Byte swapping is disabled by setting MMFF00_6 to 1.
- The correct vertical and horizontal sync polarities are specified (MMFF00_9, 10).

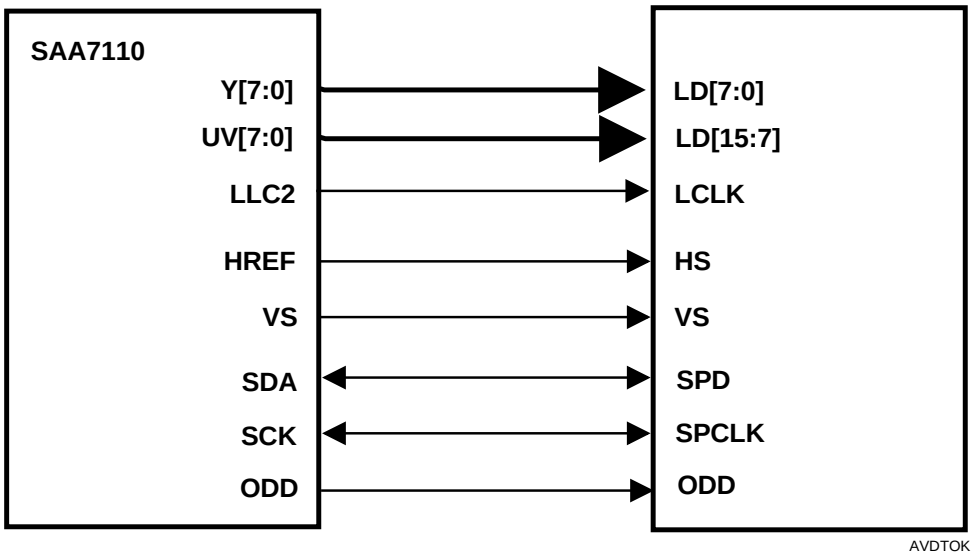


Figure 12-2. SAA7110 Digitizer Interface

- One or two frame buffer starting addresses are defined (MMFF0C, MMFF10). One is required. The second is required for double buffering.
- The horizontal and vertical decimation registers are programmed (MMFF2C, MMFF30). This is optional.
- The video input window size (height in lines and width in pixels) is programmed in MMFF24.
- The video data horizontal and vertical offsets are programmed in MMFF28.
- The line offset (stride) is programmed (MMFF34_10-0).

The SAA7110 then sends video data as shown in Figure 12-3. In this figure, both VSYNC (VS) and HSYNC (HREF) have active high polarity. The vertical offset (MMFF28_24-16) is 1, meaning the first line is skipped. The horizontal offset HO (MMFF28_11-0) is 1, meaning that the first data starts one clock after the second HREF goes low. HREF goes high again some time after the last byte of the line, whose position is specified by the line width (LW) programmed in MMFF24_11-0. The widths of the VS and HREF pulses shown may vary.

If digitizer output to a CRT or flat panel is required, alternate frames of the video input must be discarded (not written to memory) by setting bit 5 of MMFF00 to 1.

If the digitizer has an 8-bit interface, Video 8 In mode is selected by programming MMFF00_3-1 to 010b.

12.3 HOST PASS-THROUGH

When pass-through mode is enabled (MMFF00_3-1 = 100b), the CPU can write 32-bit data to the output FIFO and have this data passed directly to the decimation block (bypassing the LPB bus). The data are sent exactly as for compressed video data to an MPEG decoder. The data will then be decimated according to the programming of MMFF2C (horizontal) and MMFF30 (vertical) and then passed to the video FIFO to be written to display memory. This path is shown in Figure 12-1.

When the Host sends an HSYNC (MMFF00_12 = 1) or VSYNC (MMFF00_11), the decimation registers are re-loaded. Therefore, the Host must ensure that at least 5 clocks pass between the sync and the start of data to allow time for this reloading.

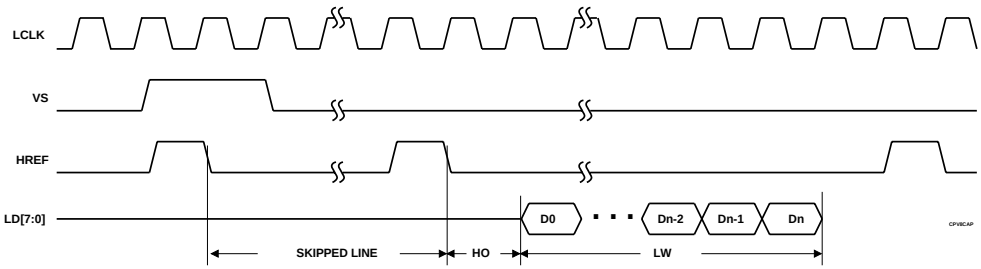


Figure 12-3. Video 8 or 16 Mode Input

Pass-through is not supported if big-endian addressing is being used.

12.4 ZV-PORT INTERFACE

The ZV-Port, or Zoomed Video Port, allows direct transmission of video data from a PC Card to ViRGE/MX. ViRGE/MX supports ZV Port operation when its LPB function is enabled (MMFF00_0 = 1) and LCLK is selected (MMFF00_24 = 1). The following setup is done for ZV Port operation:

- Video 16 mode is selected (MMFF00_3-1 = 001b)
- The ZV-Port enable bit is set (MMFF00_31 = 1)
- MMFF09_9 and MMFF00_10 must be set to 1 to specify active high HSYNC (HS) and VSYNC (VS).
- Byte swapping is disabled by setting MMFF00_6 to 1.
- One or two frame buffer starting addresses are defined (MMFF0C, MMFF10). One is required. The second is required for double buffering.
- The horizontal and vertical decimation registers are programmed (MMFF2C, MMFF30). This is optional.
- The video input window size (height in lines and width in pixels) is programmed in MMFF24.
- The video data horizontal and vertical offsets are programmed in MMFF28.
- The line offset (stride) is programmed (MMFF34_10-0).

During ZV-Port operation, ViRGE/MX automatically detects even and odd video fields based on the state of HREF on the falling edge of VS. The status of this detection is given by MMFF00_28.

The interface is shown in Figure 12-4.

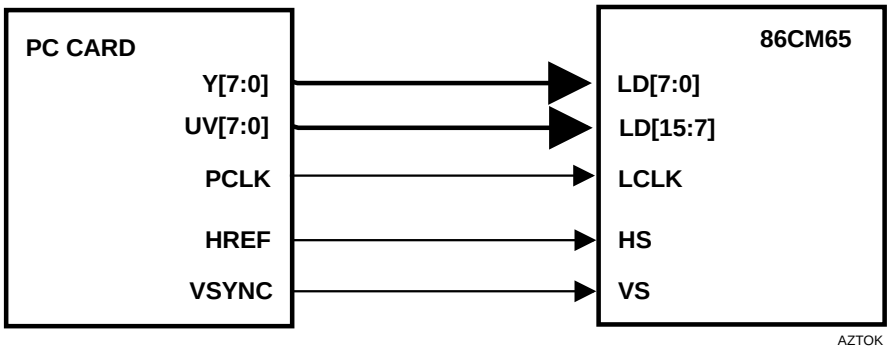


Figure 12-4. ZV Port Interface

12.5 DECIMATION

MMFF30 controls vertical decimation for all LPB inputs. There are two horizontal decimation schemes. These can be used for all inputs. The decimation scheme is selected as follows:

MMFF00_7 = 0; Use decimation scheme described for register MMFF2C
MMFF00_7 = 1; Use decimation scheme described below

In the horizontal decimation scheme described in MMFF2C, each bit in the horizontal decimation mask register corresponds to a byte in Video 8 Mode, 2 bytes in Video 16 mode and 4 bytes in pass-through mode. Any type of data could be decimated. However, this scheme does not work well with YUV or YCbCr 4:2:2 data, which are the types most often requiring decimation.

The alternate scheme works as follows:

1. Only YUV (or YCbCr) 4:2:2 data should be decimated.
2. All LPB modes use the same decimation scheme.
3. The LPB Horizontal Decimation Control register (MMFF2C) is programmed, with each bit corresponding to the Y of a YU or YV pair. A 0 specifies that the corresponding Y (luma) be kept and a 1 specifies that the corresponding Y be dropped.
4. There must be an even number of 0's (and 1's) programmed in MMFF2C so that an even number of Ys will be retained. In pass-through mode, there must be an even number of Ys in each nibble.
5. Kept Y's are paired sequentially, with each Y pair being assigned the UV pair associated with the first Y in the pair.

The operation MMFF2C is illustrated by the following example:

Mask Bit	0	1	2	3	4	5	6	7	8	9
Value	0	1	0	1	1	0	1	1	0	1
Data	Y0 U0	Y1 V0	Y2 U1	Y3 V1	Y4 U2	Y5 V2	Y6 U3	Y7 V3	Y8 U4	Y9 V4

In this example, the following Ys are kept (mask bit = 0):

Y0, Y2, Y5, Y8

Ys are paired, i.e., [Y0 Y2], [Y5 Y8]

The first Y of the first Y pair in this example is Y0. The UV pair associated with Y0 is U0 V0. Thus, the final YUV data for the first Y pair will be:
[Y0 U0 Y2 V0]
Similarly, the UV pair associated with the second Y pair in this example [Y5 Y8] will come from Y5, i.e., U2 V2, resulting in final YUV data of:
[Y5 U2 Y8 V2]

12.6 VIDEO CAPTURE

Double buffering is used for video capture. One buffer (LPB address 0) specifies the start of the even field data. The other buffer (LPB address 1) specifies the start of the odd field data. The Streams Processor buffer starting addresses must be correspondingly programmed. MM81E8_28 = 1 allows the use of separate DDA vertical accumulator initial values for the two buffers. MMFF00_30 is set to 1 to direct the incoming data to the proper buffer based on the state of the ODD input. If required, the ODD signal can be inverted before it is sampled by setting MMFF00_29 to 1. The state of the ODD signal can be read via MMFF04_20. The data from one field can be DMAed to system memory (capture) while the other field is being displayed.

12.7 VBI SUPPORT

VBI data is transmitted during vertical blanking. Capture of this data is supported by setting MMFF00_19 and MMFF00_20 to 1. The end of frame (MMFF08_2) and VSYNC trailing edge interrupts (MMFF08_7) are used to determine the timing of VBI data.

Section 13: Miscellaneous Functions

This section explains the video BIOS ROM interface, the General I/O Ports and interrupt generation.

13.1 VIDEO BIOS ROM INTERFACE

For mobile systems, the video BIOS is usually part of the system ROM. A separate ROM interface is supported for testing purposes.

The RD[7:0] (ROM data) and RA[15:0] (ROM address) signals are multiplexed on the PD[23:16] and PD[15:0] pins respectively. The $\overline{\text{ROMEN}}$ (ROM chip enable) signal is multiplexed with the FPPOL signal. $\overline{\text{ROMEN}}$ is selected when CR6F_0 = 0. The BIOS ROM must be shadowed immediately after reset (as the PCI standard requires) and BIOS access disabled to prevent interference with graphics operation.

13.2 GENERAL INPUT PORT

ViRGE/MX provides a 4-bit General Input Port (GIP) as part of its LPB function. The following steps are required to implement it.

1. Disable all other LPB uses.
2. Enable sensing of the desired input data on LD[7:4].

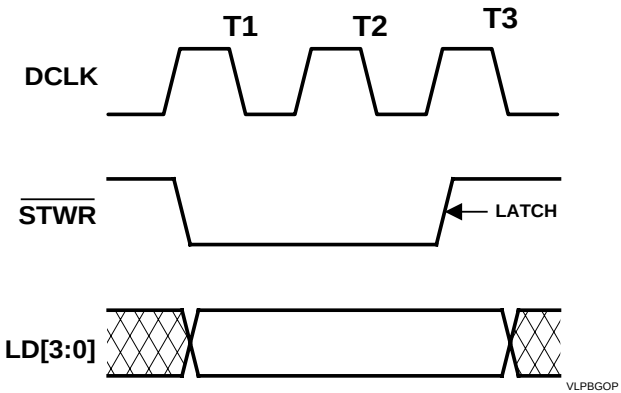


Figure 13-1. General I/O Port Timing

3. If the LPB General Output Port function is also in use, ensure that the correct output data is programmed in MMFF1C_3-0.
4. Program SR1A_4 to 1 to select $\overline{\text{STWR}}$.
5. Write (anything) to CR5C. The data on LD[7:4] are latched 2 DCLKs later into MMFF1C_7-4. (This also drives the contents of MMFF1C_3-0 onto LD[3:0] and generates the $\overline{\text{STWR}}$ pulse. The input data is latched on the rising edge of $\overline{\text{STWR}}$. See Figure 13-1)
6. Disable sensing of input data on LD[7:4].

13.3 GENERAL OUTPUT PORT

ViRGE/MX provides a 4-bit General Output Port (GOP) as part of its LPB function. To implement this:

1. Disable all other LPB uses.
2. Program the desired output in MMFF1C_3-0.
4. Program SR1A_4 to 1 to enable output of $\overline{\text{STWR}}$.
5. Write (anything) to CR5C. The data in MMFF1C_3-0 are immediately driven onto LD[3:0] and the $\overline{\text{STWR}}$ pulse is generated. The rising edge of $\overline{\text{STWR}}$ (2 DCLKs after it is asserted) can be used to latch the data into an external device. The data is held valid for 1/2 DCLK after this edge. See Figure 13-1.

ViRGE/MX also provides a 1-bit GOP on a dedicated pin. To implement this:

1. Clear SR1A_4 to 0b to select the GOP0 pin function.
2. Program the desired output in CR5C_0. This statically drives the state of CR5C_0 onto the GOP0 pin. This pin will continue to reflect the register bit states as long as SR1A_4 = 0. The value in CR5C_0 can be reprogrammed at any time.

13.4 SERIAL COMMUNICATIONS PORT

A serial communications port is implemented in the MMFF20 register. Bit 4 is set to 1 to enable the interface. The clock is written to bit 0 (= 0) and data to bit 1 (= 0), driving the SPCLK and SPD pins low respectively. The state of the SPCLK pin can be read via bit 2 and the state of the SPD pin can be read via bit 3. The SPCLK and SPD pins are tri-stated when their corresponding control bits are reset to 0, allowing other devices to drive the serial bus.

Typical uses for the serial port are for DDC monitor communications and I^2C interfacing. When SPCLK and SPD are tri-stated, ViRGE/MX can detect an I^2C start condition (SPD driven low while SPCLK is not driven low). This condition is generated by another I^2C master that wants control of the I^2C bus. If bit 19 of MMFF08 is set to 1, detection of a start condition generates an interrupt and sets bit 3 of MMFF08 to 1. If bit 24 of MMFF08 is set to 1, ViRGE/MX drives SPCLK low to generate I^2C wait states until the Host can clear the interrupt and service the I^2C bus.

If PD26 is strapped low at reset, strapping of PD25 selects either E2H (PD25 pulled high) or E8H (PD25 pulled low) as the I/O port address for the Serial Port register. This allows the ports to be used for serial communications, typically I^2C, even when ViRGE/MX is not enabled.

13.5 INTERRUPT GENERATION

Whatever the mode of operation (VGA or Enhanced), bit 4 of CR32 must be set to 1 to enable interrupt generation. When an enabled interrupt is generated, $\overline{\text{INTA}}$ is pulled low.

When ViRGE/MX is being operated in VGA mode (CR66_0 = 0), only a vertical retrace can generate an interrupt. This is enabled when CR11_5 = 0 and CR11_4 = 1. When an interrupt occurs, it is cleared by writing a 0 to CR11_4. The interrupt must then be re-enabled by writing a 1 to the same bit. Note that the BIOS clears both bit 4 and bit 5 of CR11 to 0 during power-on, a mode set or a reset. Thus, interrupt generation is disabled until bit 4 is set to 1.

When ViRGE/MX is being operated in Enhanced mode (CR66_0 = 1), interrupts can be generated by a vertical retrace, S3d Engine done, command FIFO overflow, command FIFO empty, host DMA done, command DMA doneand S3d FIFO empty. These interrupts are enabled and cleared and their status reported via MM8504. LPB and serial port interrupts are controlled via MMFF08. If interrupts are used, they should be cleared before they are enabled.

Multiple interrupts can be enabled at the same time in Enhanced mode. The interrupt pin will remain asserted until all interrupt status bits are cleared.

Section 14: Basic Software Functions

This section describes some of the basic operations required to program ViRGE/MX.

14.1 CHIP WAKEUP

The following program wakes up ViRGE/MX. This is required for systems that do not use the S3 style of video BIOS, e.g, UNIX.

```
mov dx,3c3h       ; Video Subsystem Enable register address
mov al,01h        ; bit 0 = 1, enable graphics display
out dx,al         ; write new bit values to 3c3h
mov dx,3cch       ; Miscellaneous Output Read register
in al,dx          ; Read 3cch
[load CRTCs]      ; program CRTC registers
mov dx,3C6h       ; DAC Mask register address
mov al,FFh        ; DAC Mask register initialization value
out dx,al         ; Initialize DAC mask and release BLANK signal
  .
  .
  .
```

14.2 REGISTER ACCESS

S3 has added a number of graphics registers to the standard VGA set. These can be locked when not in use to prevent accidental access and unlocked when access is required. This section explains how this is done.

14.2.1 Unlocking the S3 Registers

The S3 registers (CR30 and higher plus the Enhanced Commands registers) must be unlocked before they can be accessed by the CPU. The code to do this is:

Note: Byte operations are used in the following examples for clarity. Word operations, e.g.,

```
mov ax, 4838h
out dx,ax
```

should be used for efficiency instead of the operations used in the first example below.

```
; Write code to SR8 to provide access to the S3 extended Sequencer registers
(SR9-SRFF)
;
   mov dx,3c4h       ; copy index register address into dx
   mov al,08h        ; copy index for SR8 register into al
   out dx,al         ; write index to index register
   inc dx            ; increment dx to 3c5h (data register address)
   mov al,06h        ; copy unlocking code (xxxx0110b, x=don't care) to al
   out dx,al         ; write the unlocking code to the data register
   dec dx            ; restore the index register address to dx
;
; Write code to CR38 to provide access to extended CRTC registers CR2D-CR3F
;
   mov dx,3d4h       ; copy index register address into dx
   mov al,38h        ; copy index for CR38 register into al
   out dx,al         ; write index to index register
   inc dx            ; increment dx to 3D5h (data register address)
   mov al,48h        ; copy unlocking code (01xx10xxb, x=don't care) to al
   out dx,al         ; write the unlocking code to the data register
   dec dx            ; restore the index register address to dx
;
; Write code to CR39 to provide access to extended CRTC registers CR40-CRFF
;
; dx is already loaded with 3D4h because of the previous instruction
;
   mov al,39h        ; copy index for CR39 register into al
   out dx,al         ; write index to index register
   inc dx            ; increment dx to 3D5h (data register address)
   mov al,0a5h       ; copy unlocking code to al (the code a5H also unlocks
                     ; access to configuration registers CR36, CR37 and CR68
   out dx,al         ; write the unlocking code to the data register
   dec dx            ; restore the index register address to dx
;
```

14.2.2 Locking the S3 Registers

Relocking the S3 registers is done by repeating the code used to unlock the registers except:

1. The values written to the SR8, CR38 and CR39 registers must change at least one of the significant bits in the valid code pattern. For example, 00h will always accomplish this.

2. After first verifying that the Graphics Engine is not busy (bit 9 of 9AE8H is 0), bit 0 of CR40 must be cleared to 0. A read-modify-write cycle must be used instead of the code used above to prevent overwriting of any changes made to bits 7-1 in CR40 since reset.

```
mov dx,3d4h       ; copy index register address into dx
mov al,40h        ; copy index for CR40 register into al
out dx,al         ; write index to index register
inc dx            ; increment dx to 3D5h (data register address)
in al,dx          ; read content of CR40 into al
and al,0feh       ; clear bit 0 to 0
out dx,al         ; write to CR40 to lock the Enhanced Commands registers
dec dx            ; restore the index register address to dx
```

14.3 TESTING FOR THE PRESENCE OF A ViRGE/MX CHIP

After unlocking, a ViRGE/MX chip can be identified via CR2D and CR2E.

```
mov dx,3d4h       ; copy index register address into dx
mov al,2dh        ; copy index for CR2D register into al
out dx,al         ; write index to index register
inc dx            ; increment dx to 3D5h (data register address)
in al,dx          ; read content of CR2D into al
cmp al,8ch        : compare chip ID to the desired chip ID high (8ch)
jne not_8c        ; jump to a label if chip ID does not match desired ID
mov dx,3d4h       ; copy index register address into dx
mov al,2eh        ; copy index for CR2E register into al
out dx,al         ; write index to index register
inc dx            ; increment dx to 3D5h (data register address)
in al,dx          ; read content of CR2E into al
cmp al,01h        : compare chip ID to the desired chip ID low (01h)
jne not_01        ; jump to a label if chip ID does not match desired ID
.                 ; ViRGE/MX found - continue with setup
.
.
```

A ViRGE/MX+ chip is identified by 8CH in CR2D and 04H in CR2E.

Specific revisions of the chip can be identified via CR2F. The PCI configuration space device and revision ID fields can also be used to identify the chip.

14.4 GRAPHICS MODE SETUP

Some programs may require a graphics mode other than that provided by standard operation. For example, a DOS game may require a resolution of 640x400x8 (VESA mode 100) instead of the standard DOS mode, e.g., mode 03. The following code fragment shows how this is done.

```
mov ax,4f02h      ; VESA super VGA mode function call
mov bx,100h       ; mode 100
int 10h           ; call video BIOS
```

Section 15: Enhanced Programming

Enhanced mode provides a level of performance far beyond what is possible with the VGA architecture. Hardware BitBLTs (with 256 ROPs), 2D and 3D line drawing, 2D polygon fills and 3D triangle drawing are implemented. Hardware cursor support and clipping are also supported. While in Enhanced mode, the display memory bit map can be updated in two ways. One is to have the CPU issue commands and send data to the S3d Engine, which then controls pixel updating. The other is to have the CPU write directly to memory. (This is also possible in non-Enhanced modes.) This section explains these two methods and provides a set of Enhanced mode 2D programming examples and explains the basic elements of 3D drawing.

15.1 MEMORY-MAPPED I/O

ViRGE/MX provides two memory-mapped I/O (MMIO) methods. For the "old" method, the base address is A000H (or B800H), allowing use during DOS and real mode operation. For the "new" method, the base address is the linear addressing (or PCI) base address and requires protected mode. In addition, address space is provided for linear addressing and big endian addressing. Each of these MMIO methods is described below.

15.1.1 Old MMIO

Setting bits 4-3 of CR53 to 10b enables the old MMIO function. A setting of 11b enables both the old and new MMIO methods simultaneously. When the old MMIO is enabled, CR53_5 selects the base address. CR53_5 = 0 places the MMIO window at A0000H - AFFFFH. CR53_5 = 1 places the MMIO window at B8000H - BFFFFH. The latter setting leaves A0000H - B7FFFH free for VGA memory and other uses. In either case, all ViRGE/MX registers are accessible via either window at the variable offsets shown in Table 15-1. For example, the PCI configuration space registers are found starting at A8000H (or B8000H, depending on the setting of CR53_5).

With old MMIO enabled and CR53_5 =0, image writes are made by accessing any memory location in the 32-KByte address space from A0000H to A7FFFH. This allows efficient use of the MOVSW and MOVSD assembly language commands. Accesses must be to doubleword addresses. Software must not make image writes beyond the A7FFFH range. If CR53_5 = 1, image writes cannot be made as the A0000H - A7FFFH range is reserved.

When MMIO is enabled (old or new), clearing bit 7 of SR9 to 0 allows both programmed I/O (IN, OUT) access and MMIO (MOV) access. Setting this bit to 1 disables programmed I/O access, allowing only MMIO access. The latter is required for plug and play operation.

15.1.2 New MMIO

The new MMIO method for ViRGE/MX provides a 64-MByte addressing window starting at the base address specified in CR59-5A or the PCI base address register. This space is divided into a 32-MByte space for little endian (Intel-style) addressing and a 32-MByte space for big endian (Power PC-style) addressing. All registers and data transfer locations are mapped into this area as shown in Table 15-1.

The new MMIO (only) is enabled by setting bits 4-3 of CR53 to 01b. This is the default, allowing PCI software immediate access to all registers and the ability to relocate the address space. The new MMIO is also enabled in conjunction with the old MMIO method when bits 4-3 of CR53 are set to 11b.

When MMIO is enabled (old or new), clearing bit 7 of SR9 to 0 allows both programmed I/O (IN, OUT) access and MMIO (MOV) access. Setting this bit to 1 disables programmed I/O access, allowing only MMIO access. The latter is required for plug and play operation.

Table 15-1. New MMIO Addresses

Lower 32 MBytes - Little Endian Addressing	
Description	**Offset From Base (Hex)**
Linear Addressing (16M)	000 0000 - 0FF FFFF
Image Data Transfer (32K)	100 0000 - 100 7FFF
PCI Configuration Space Registers	100 8000 - 100 8043
Streams Processor Registers	100 8180 - 100 81FF
Memory Port Controller	100 8200 - 100 8224
CRT VGA 3B? Registers	100 83B0 - 100 83Bx
CRT VGA 3C? Registers	100 83C0 - 100 83Cx
CRT VGA 3D? Registers	100 83D0 - 100 83Dx
Subsystem Status Enhanced Register	100 8504
Advanced Function Control Register	100 850C
DMA Controller Registers	100 8580 - 100 85FF
Color Pattern Registers	100 A000 - 100 A1FF
BitBLT/Rectangle Fill Registers	100 A400 - 100 A5FF
2D Line Draw Registers	100 A800 - 100 A9FF
2D Polygon Fill Registers	100 AC00 - 100 ADFF
3D Line Draw Registers	100 B000 - 100 B1FF
3D Triangle Registers	100 B400 - 100 B5FF
Local Peripheral Bus Registers	100 FF00 - 100 FF5C

Values in the gaps between the memory ranges shown in Table 15-1 are reserved.

For big endian addressing, add 2 to the most significant hex digit shown in Table 15-1, i.e., 0xx xxxx becomes 2xx xxxx and 1xx xxxx becomes 3xx xxxx. Thus, the total address space decoded by ViRGE/MX is 64 MBytes.

15.2 DIRECT BITMAP ACCESSING—LINEAR ADDRESSING

Linear addressing is useful when software requires direct access to display memory. ViRGE/MX provides two linear addressing schemes. The old method can be used when MMIO is disabled or with the old MMIO method. The second is used in conjunction with the new MMIO method.

15.2.1 Old Linear Addressing

ViRGE/MX provides linear addressing of up to 4 MBytes of display memory. Linear addressing of more than 64 KBytes requires that the CPU be operated in protected mode. To use linear addressing in non-Enhanced modes, CR66_6 must be set to 1.

The S3d Engine busy flag, bit 13 of MM8504 (read), should be verified to be 0 (not busy) before linear addressing is enabled by setting bit 4 of CR58 to 1. The size of the linear address window is set via bits 1-0 of CR58. The base address for the linear addressing window is set via CR59 and CR5A (or via the Base Address 0 (Index 10H) PCI configuration register for PCI systems).

For operation in real mode, the linear addressing window size can be set to 64 KBytes. The base address for the window is set to A0000H by programming bits 31-16 of the window position in CR59-CR5A to 000AH. If bit 0 of CR31 is set to 1, the memory page offset (64K bank) specified in bits 5-0 of CR6A is added to the linear addressing window position base address, allowing access to up to 4 MBytes of display memory through a 64-KByte window.

15.2.2 New Linear Addressing

With the new MMIO enabled (CR53_4-3 = 01b or 11b), the first 16 MBytes of each 32M address space (big and little endian) are dedicated to linear addressing. A maximum of 4 MBytes of each address space (starting at the lowest address of the space) is usable with ViRGE/MX. The base address is taken from bits 31-26 of the linear address window position (bits 7-2 of CR59 or the high order 6 bits of the the PCI Base Address 0). This is concatenated with the display memory address specified by the programmer.

In addition to enabling the new MMIO, the programmer must also enable linear addressing and specify the window size exactly as required for the old linear addressing. Note that since only bits 31-26 are used to specify the base address, A0000H cannot be specified and the 64K banking scheme possible with the old linear addressing cannot be used with the new linear addressing.

When big endian addressing is used, the required byte swapping for linear addressing is specified by bits 2-1 of CR53. This applies to both reads and writes.

15.3 READ AND WRITE ORDERING

An overview of the ViRGE/MX internal organization is shown in Figure 15-1. Note that there are three independent and concurrent paths for communications between the CPU and ViRGE/MX registers and memory. The time required for any given read or write to complete (latency) varies by path. This can have important implications for the programmer.

First is the issue of write ordering. For example, a linear addressing write to memory uses the command FIFO path, while an image write to memory uses the S3d FIFO path. If the programmer issues a linear addressing command and then an image write command before the linear address command completes (or vise versa), there is no guarantee which will complete first. For total safety from prematurely overwriting memory data, the programmer must check that the S3d FIFO is empty before doing linear addressing updating or for command FIFO empty before doing an image transfer.

Similarly, if correct operation of any command is dependent on operation using another FIFO path (such as a VGA register update before an S3d command), the programmer must ensure that the relevant FIFO is empty before issuing the dependent command.

Reads through the LPB and VGA paths bypass the respective FIFOs. However, they will be held until the relevant FIFO is empty before completing. For PCI systems, this will generate a disconnect (if bit 3 of CR66 is set to 1). This hold guarantees that a read of a register following a write will yield the correct data. Reads of S3d registers go through the S3d FIFO. However, any read with the S3d FIFO not empty or with the S3d Engine busy will yield undefined results.

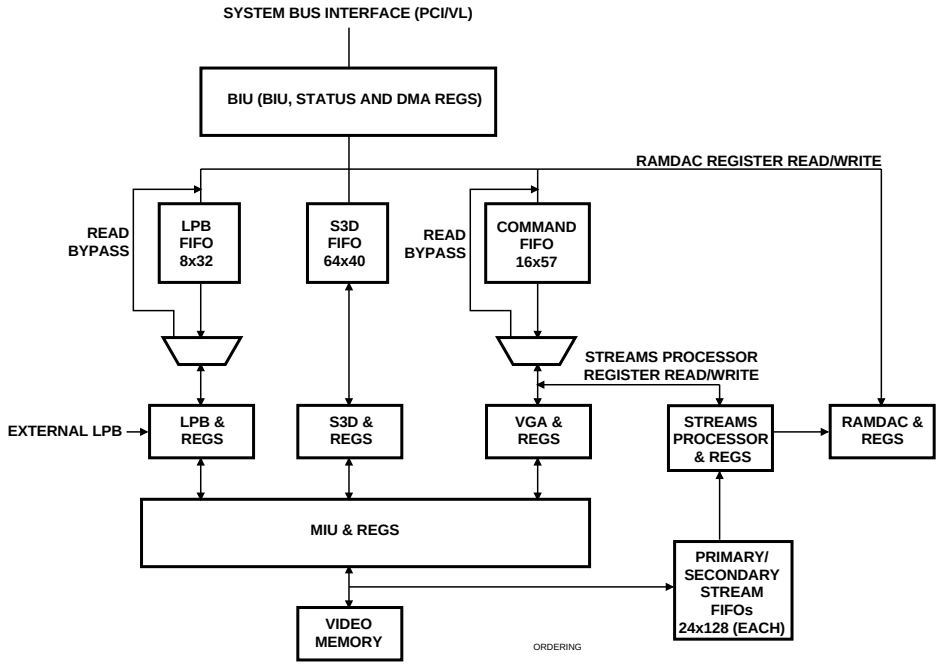


Figure 15-1. Internal Organization

15.4 S3d ENGINE PROGRAMMING

All Enhanced mode programming should be done using memory-mapped I/O.

MMIO Format:

Enable MMIO
Point ES to A000H (old MMIO) or base address (new MMIO)
Load the x and y values into EAX (y value in the low word and x value in the high word), I.e.,

EAX ⇐ x,y

MOV ES:[REGMNEMONIC], EAX

The MMIO scheme is the most efficient and is used where appropriate in the programming examples provided later in this section. All assume that the ES register points to A000H is the old MMIO is being used or the base address if the new MMIO is being used.

15.4.1 Notational Conventions

The following provides examples of the conventions used in the programming examples. Text following a ';' is a comment.

ES:[MMXXXX] ⇐ BN1 (bh-bl), BN2 (bh-bl)

MMXXXX identifies the memory-mapped register, with XXXX being the variable part of the address offset. Thus MMA504 identifies the register at offset 100 A504H. BN1 (bh-bl) represents a bit mnemonic followed by the bit location(s). Thus, SRC_X (26-16) indicates that the Source X value is programmed into bits 26-16.

The complete binary programming of the Command Set register is provided. For example,

ES:[MM????] ⇐ XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX Where:

???? = appropriate variable offset value for the Command Set register, e.g., A500 for BitBLTs.
X = 0; bit value = 0
X = 1; bit value = 1
X = S; this bit value must be specified, but can vary for this command

Image transfers (CPU pixel data writes to the frame buffer) are notated as follows:

COUNT
IMAGEDATA ⇐ RECT_DATA

The COUNT is the number of CPU writes. IMAGEDATA means the 32K Image Data Transfer memory space at the memory-mapped location shown in Table 15-1.

15.4.2 Initial Setup

All examples assume the desired mode is selected.

If bit 1 of the Command Set register is set to 1, all bitmap updates are affected by the settings in the clipping registers (MMxxDC, MMxxE0).

15.4.3 Autoexecute

When bit 0 of the Command Set register is cleared to 0, the command is executed when the Command Set register is written. If this bit is set to 1, the command is not executed until the register with the highest address for that command type (BitBLT, Line Draw, etc.) is written. This allows multiple executions of a given command using different parameters without re-programming the Command Set register. Full programming examples for autoexecute on are provided for each command type.

15.4.4 2D Programming Examples

This section provides programming examples for the following Enhanced mode 2D drawing operations:

- BitBLT
- Rectangle Fill
- 2D Line Draw
- 2D Polygon Fill

15.4.4.1 BitBLT

The BitBLT function provides a full implementation of the 256 raster operations as defined by Microsoft for Windows. A listing and explanation of these is provided in Appendix A.

Each raster op has three operands: Source, Pattern and Destination. The Source pixel can be from the screen (current bitmap) or from the CPU (image transfer). When the source is the screen, the pixel depth is always the same for both the source and destination (8, 16, 24 bits/pixel). When the source is the CPU, the pixel can be either color (same source and destination pixel depth) or mono (1 bit/pixel).

The Pattern is an 8x8 array of pixels. A mono pattern is specified in the Mono Pattern 0 and 1 registers. The Pattern Foreground and Background Color registers define the pixel colors. A color pattern is specified in a set of registers starting at offset 100 A100H. The number of registers required depends on the color depth.

The Destination pixel is always the screen (current bitmap) and is always color (multi bits/pixel). This is the pixel that will be overwritten or left unchanged by the result of the operation.

Based on the above definitions, there are 6 valid BitBLT cases:

Color Pattern

- Source = Screen, Color Pixels
- Source = CPU, Color Pixels
- Source = CPU, Mono Pixels

Mono Pattern

- Source = Screen, Color Pixels
- Source = CPU, Color Pixels
- Source = CPU, Mono Pixels

When the source and destination are overlapping rectangles on the screen , care must be taken so that the source data is not overwritten before it is moved. This issue is explained next, followed by programming examples for each of these above cases.

Overlapping Rectangles Case

Figure 15-2 shows the 4 cases for overlapping rectangles. Table 15-2 gives the proper programming parameters for each case. The direction indicates the order in which the pixels are moved, from left to right (X+) or right to left (X-) and top to bottom (Y+) or bottom to top (Y-). These are specified via bits 25 and 26 of the Command Set register. The source and destination coordinates are specified via the Rectangle Source XY and Rectangle Destination XY registers. x1,Y1 is the pixel position of the upper left hand corner of the source rectangle. x2,Y2 is the pixel position of the upper left hand corner of the destination rectangle. The width of the rectangle is W (in pixels) and the height is H (in lines). As indicated in the figure, you always start with the source corner inside the overlap and move that pixel to the corresponding corner for the destination pixel.

Table 15-2 Programming Parameters for Overlapping BitBLTs

Case	Direction	SRC_X	SRC_Y	DEST_X	DEST_Y
1	X+, Y+	x1	y1	x2	y2
2	X-, Y-	x1 + W - 1	y1 + H -1	x2 + W - 1	y2 + H -1
3	X-, Y+	x1 + W - 1	y1	x2 + W - 1	y2
4	X+, Y-	x1	y1 + H -1	x2	y2 + H -1

The basic algorithm is if the drawing direction is negative, add [rectangle dimension -1] in that direction to the normal source/destination location. If the drawing direction is positive, use the original source/destination location.

The parameters for Case 1 are appropriate for non-overlapping rectangles.

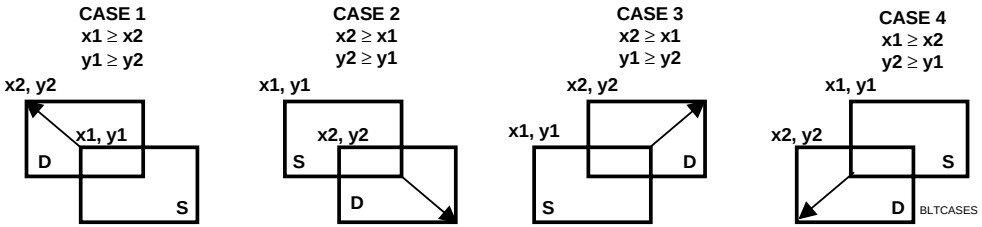


Figure 15-2. Overlapping BitBLT Cases

Color Pattern Case 1 (Source = Screen, Color Pixels)

This command copies a source rectangular area in display memory to another location in display memory. The 8x8 pixel pattern is programmed in the color pattern registers. For this example, assume x1,y1 is the top left corner of the source rectangle in display memory and x2,y2 is the top left corner of the destination rectangle. The rectangles can be overlapping or disjoint. See Table 15-2 for the source and destination coordinate parameter values for overlapping cases. The height and width (in pixels) of the rectangle being copied are H and W. The color depth is assumed to be 8 bits/pixel.

Autoexecute Off:

```
ES:[MMA100] ⇐ P3 (31-24), P2 (23-16), P1 (15-8), P0 (7-0)        ; Pixels 3-0 of the color pattern
  .
  .
  .
ES:[MMA13C] ⇐ P63 (31-24), P62 (23-16), P61 (15-8), P60 (7-0)    ; pixels 63-60 of the color pattern
ES:[MMA504] ⇐ W-1 (26-16), H (10-0)                              ; rectangle width and height
ES:[MMA508] ⇐ SRC_X (26-16), SRC_Y (10-0)                        ; source x and y start coordinates
ES:[MMA50C] ⇐ DEST_X (26-16), DEST_Y (10-0)                      ; destination x and y start coord.
ES:[MMA500] ⇐ 0000 0SSS SSSS SSS0 0000 0000 0010 00S0            ; Command Set register
```

The following must be specified: Y direction (bit 26), X direction (bit 25), ROP (bits 24-17), clipping enable (bit 1). Bits 4-2 will be different for other color depths.

Autoexecute On:

```
ES:[MMA100] ⇐ P3 (31-24), P2 (23-16), P1 (15-8), P0 (7-0)        ; pixels 3-0 of the color pattern
  .
  .
  .
ES:[MMA13C] ⇐ P63 (31-24), P62 (23-16), P61 (15-8), P60 (7-0)    ; pixels 63-60 of the color pattern
ES:[MMA500] ⇐ 0000 0SSS SSSS SSS0 0000 0000 0010 00S1            ; bit 0 = 1 for autoexecute
ES:[MMA504] ⇐ W-1 (26-16), H (10-0)                              ; rectangle width and height
ES:[MMA508] ⇐ SRC_X (26-16), SRC_Y (10-0)                        ; source x and y start coordinates
ES:[MMA50C] ⇐ DEST_X (26-16), DEST_Y (10-0)                      ; destination x and y start coord.
```

The command is executed when MMA50C is programmed. The order of programming the other registers is not important. With autoexecute on, additional BitBLTs can be performed by reprogramming only the parameter registers (not the Command Set register), always ending with the Rectangle Destination XY register (MMA50C).

Color Pattern Case 2 (Source = CPU, Color Pixels)

This command transfers a rectangular color image provided by the CPU to a location in display memory. The 8x8 pixel pattern is programmed in the color pattern registers. For this example, assume the height and width (in pixels) of the rectangle being copied are H and W. The color depth is assumed to be 8 bits/pixel.

Autoexecute Off:

```
ES:[MMA100] ⇐ P3 (31-24), P2 (23-16), P1 (15-8), P0 (7-0)          ; pixels 3-0 of the color pattern
  .
  .
  .
ES:[MMA13C] ⇐ P63 (31-24), P62 (23-16), P61 (15-8), P60 (7-0)      ; pixels 63-60 of the color pattern
ES:[MMA504] ⇐ W-1 (26-16), H (10-0)                                ; rectangle width and height
ES:[MMA50C] ⇐ DEST_X (26-16), DEST_Y (10-0)                        ; destination x and y start coord.
ES:[MMA500] ⇐ 0000 000S SSSS SSS0 00SS SS00 1010 00S0              ; Command Set register
```

The following must be specified: ROP (bits 24-17), first dword offset (bits 13-12), image transfer alignment (bits 11-10), clipping enable (bit 1). Bits 4-2 will be different for other color depths.

```
COUNT (of image pixel data to transfer) = (See Note)
IMAGEDATA ⇐ RECT_DATA              ; Output data to Image Transfer addresses for COUNT dwords
```

Autoexecute On:

Writing to the Destination XY register (MMA50C) executes the command.

Note

If the CPU obtains the image data from a source bitmap written to system memory by the application, the application passes the origin of this bitmap, its width, height and color depth. Some or all of this bitmap can then be blitted to display memory (screen). The method of transfer varies depending on whether or not the entire bitmap or a partial bitmap is transferred.

For source bitmaps from an application, each line is required by specification to be word aligned, i.e., data for a new line begins with the next word after the last word containing valid data for the previous line. Therefore, to transfer a complete source bitmap, the driver does the following:

1. All image transfers must be doubleword aligned. Therefore, bits 13-12 of the Command Set register must be programmed to properly reflect the alignment of the first pixel of the source bitmap. For example, if the first pixel of the source bitmap starts with the third byte of the first doubleword-aligned read, bits 13-12 of the Command Set register must be programmed to 10b to tell the Engine to ignore the first two bytes.
2. Word alignment must be specified by programming bits 11-10 of the Command Set register to 01b. This tells the Engine that the data for the next line starts at the next word after the data ending the line. In some cases, doubleword alignment is appropriate (bits 11-10 of the Command set register = 10b). This is more efficient, but is a special case. Word alignment always works.
3. To determine the number of doublewords to transfer, calculate (for the source bitmap):

   int [(width x height x bits/pixel) + 31]/32.

4. The image transfer area in memory is 32K (offset 100 0000H - 100 7FFFH). The driver must monitor the addresses for image writes and reset the address pointer back to the start before any writes are made beyond the 32K area.

If the application requests that only a rectangular subsection of the source bitmap be transferred to display memory, the driver has multiple choices of how to do this.

1. The driver can transfer the entire source bitmap and use the clipping registers to eliminate the unwanted pixels.
2. The driver can transfer only the requested pixels, but it must do this one line at time. If the start of each line is not doubleword aligned, the driver must determine the doubleword address containing the first data for the first line and the number of doublewords required to send the whole line. It must then issue the command to blit this line, with bits 13-12 of the Command Set register set to ignore the appropriate number of bytes at the start of the line. The driver must then change the address to the start of the next line and repeat the above process, including specification of a new destination start address. The result is that one command is executed for each line.

   Note that if the lines for the requested pixels happen to start at doubleword addresses, the entire rectangle can be blitted with a single command because no data needs to be ignored at the start of each line. The driver still needs to keep track of the line length and increment the address by the stride at the end of each line.
3. The driver can transfer the requested pixels as described in 2 above and use the clipping registers to eliminate any extra pixels at the start of each line.

Color Pattern Case 3 (Source = CPU, Mono Pixels)

This command transfers a rectangular mono image provided by the CPU to a location in display memory. The mono image is converted to the screen color depth based on the the pattern color (potentially) mixed with the screen (destination) color. The 8x8 pixel pattern is programmed in the color pattern registers. For this example, assume the height and width (in pixels) of the rectangle being copied are H and W. The screen color depth is assumed to be 8 bits/pixel.

Autoexecute Off:

```
ES:[MMA100] ⇐ P3 (31-24), P2 (23-16), P1 (15-8), P0 (7-0)          ; pixels 3-0 of the color pattern
  .
  .
  .
ES:[MMA13C] ⇐ P63 (31-24), P62 (23-16), P61 (15-8), P60 (7-0)      ; pixels 63-60 of the color pattern
ES:[MMA504] ⇐ W-1 (26-16), H (10-0)                                ; rectangle width and height
ES:[MMA50C] ⇐ DEST_X (26-16), DEST_Y (10-0)                        ; destination x and y start coord.
ES:[MMA500] ⇐ 0000 000S SSSS SSS0 00SS SS00 1110 00S0              ; Command Set register
```

The following must be specified: ROP (bits 24-17), first dword offset (bits 13-12), image transfer alignment (bits 11-10), clipping enable (bit 1). Bits 4-2 will be different for other color depths.

```
COUNT (of image pixel data to transfer) = (See Note)
IMAGEDATA ⇐ RECT_DATA              ; Output data to Image Transfer addresses for COUNT dwords
```

Autoexecute On:

Writing to the Destination XY register (MMA50C) executes the command.

Note

If the source bitmap is provided by the application, then the entire Note for the previous color pixels case also applies to this mono pixel case because each line is required to be word aligned. If the source bitmap is provided by the driver, e.g., font data, the driver should byte align the data and program bits 11-10 of the Command Set register to 00b to specify byte alignment to the Engine.

Mono Pattern Case 1 (Source = Screen, Color Pixels)

This command copies a source rectangular area in display memory to another location in display memory. It is identical to the Color Pattern Case 1 except that the 8x8 pixel pattern is programmed in the mono pattern registers and the pattern color is taken from the pattern foreground and background registers. For this example, assume x1,y1 is the top left corner of the source rectangle in display memory and x2,y2 is the top left corner of the destination rectangle. The rectangles can be overlapping or disjoint. See Table 15-2 for the source and destination coordinate parameter values for overlapping cases. The height and width (in pixels) of the rectangle being copied are H and W. The screen color depth is assumed to be 8 bits/pixel.

Autoexecute Off:

```
ES:[MMACE8] ⇐ MONO PATTERN 0                              ; 1st 32 bits of mono pattern
ES:[MMACEC] ⇐ MONO PATTERN 0                              ; 2nd 32 bits of mono pattern
ES:[MMACF0] ⇐ DATA1 (7-0)                                 ; 8-bit pattern backgnd color index
ES:[MMACF4] ⇐ DATA1 (7-0)                                 ; 8-bit pattern foregnd color index
ES:[MMA504] ⇐ W-1 (26-16), H (10-0)                       ; rectangle width and height
ES:[MMA508] ⇐ SRC_X (26-16), SRC_Y (10-0)                 ; source x and y start coordinates
ES:[MMA50C] ⇐ DEST_X (26-16), DEST_Y (10-0)               ; destination x and y start coord.
ES:[MMA500] ⇐ 0000 0SSS SSSS SSS0 0000 0001 0010 00S0     ; Command Set register
```

The following must be specified: Y direction (bit 26), X direction (bit 25), ROP (bits 24-17), clipping enable (bit 1). Bits 4-2 and the fields programmed for the background and foreground colors will be different for other color depths.

Autoexecute On:

Writing to the Destination XY register (MMA50C) executes the command.

Mono Pattern Case 2 (Source = CPU, Color Pixels)

This command transfers a rectangular color image provided by the CPU to a location in display memory. It is identical to the Color Pattern Case 1 described earlier except that the 8x8 pixel pattern is programmed in the mono pattern registers and the pattern color is taken from the pattern foreground and background registers. For this example, assume the height and width (in pixels) of the rectangle being copied are H and W. The screen color depth is assumed to be 8 bits/pixel.

Autoexecute Off:

```
ES:[MMACE8] ⇐ MONO PATTERN 0                              ; 1st 32 bits of mono pattern
ES:[MMACEC] ⇐ MONO PATTERN 0                              ; 2nd 32 bits of mono pattern
ES:[MMACF0] ⇐ DATA1 (7-0)                                 ; 8-bit pattern backgnd color index
ES:[MMACF4] ⇐ DATA1 (7-0)                                 ; 8-bit pattern foregnd color index
ES:[MMA504] ⇐ W-1 (26-16), H (10-0)                       ; rectangle width and height
ES:[MMA508] ⇐ SRC_X (26-16), SRC_Y (10-0)                 ; source x and y start coordinates
ES:[MMA50C] ⇐ DEST_X (26-16), DEST_Y (10-0)               ; destination x and y start coord.
ES:[MMA500] ⇐ 0000 000S SSSS SSS0 0001 1001 0010 00S0     ; Command Set register
```

The following must be specified: ROP (bits 24-17), first dword offset (bits 13-12), image transfer alignment (bits 11-10), clipping enable (bit 1). Bits 4-2 will be different for other color depths.

Autoexecute On:

```
COUNT (of image pixel data to transfer) = (See Note)
IMAGEDATA ⇐ RECT_DATA          ; Output data to Image Transfer addresses for COUNT dwords
```

Autoexecute On:

Writing to the Destination XY register (MMA50C) executes the command.

Note

If the CPU obtains the image data from a source bitmap written to system memory by the application, the application passes the origin of this bitmap, its width, height and color depth. Some or all of this bitmap can then be blitted to display memory (screen). The method of transfer varies depending on whether or not the entire bitmap or a partial bitmap is transferred.

For source bitmaps from an application, each line is required by specification to be word aligned, i.e., data for a new line begins with the next word after the last word containing valid data for the previous line. Therefore, to transfer a complete source bitmap, the driver does the following:

1. All image transfers must be doubleword aligned. Therefore, bits 13-12 of the Command Set register must be programmed to properly reflect the alignment of the first pixel of the source bitmap. For example, if the first pixel of the source bitmap starts with the third byte of the first doubleword-aligned read, bits 13-12 of the Command Set register must be programmed to 10b to tell the Engine to ignore the first two bytes.
2. Word alignment must be specified by programming bits 11-10 of the Command Set register to 01b. This tells the Engine that the data for the next line starts at the next word after the data ending the line. In some cases, doubleword alignment is appropriate (bits 11-10 of the Command set register = 10b). This is more efficient, but is a special case. Word alignment always works.

3. To determine the number of doublewords to transfer, calculate (for the source bitmap):

   int [(width x height x bits/pixel) + 31]/32.

4. The image transfer area in memory is 32K (offset 100 0000H - 100 7FFFH). The driver must monitor the addresses for image writes and reset the address pointer back to the start before any writes are made beyond the 32K area.

If the application requests that only a rectangular subsection of the source bitmap be transferred to display memory, the driver has multiple choices of how to do this.

1. The driver can transfer the entire source bitmap and use the clipping registers to eliminate the unwanted pixels.
2. The driver can transfer only the requested pixels, but it must do this one line at time. If the start of each line is not doubleword aligned, the driver must determine the doubleword address containing the first data for the first line and the number of doublewords required to send the whole line. It must then issue the command to blit this line, with bits 13-12 of the Command Set register set to ignore the appropriate number of bytes at the start of the line. The driver must then change the address to the start of the next line and repeat the above process, including specification of a new destination start address. The result is that one command is executed for each line.

   Note that if the lines for the requested pixels happen to start at doubleword addresses, the entire rectangle can be blitted with a single command because no data needs to be ignored at the start of each line. The driver still needs to keep track of the line length and increment the address by the stride at the end of each line.
3. The driver can transfer the requested pixels as described in 2 above and use the clipping registers to eliminate any extra pixels at the start of each line.

Mono Pattern Case 3 (Source = CPU, Mono Pixels)

This command transfers a rectangular mono image provided by the CPU to a location in display memory. The mono image is converted to the screen color depth based on the the pattern color (potentially) mixed with the screen (destination) color. It is identical to the Color Pattern Case 3 described earlier except that the 8x8 pixel pattern is programmed in the mono pattern registers and the pattern color is taken from the pattern foreground and background registers. For this example, assume the height and width (in pixels) of the rectangle being copied are H and W. The screen color depth is assumed to be 8 bits/pixel.

Autoexecute Off:

```
ES:[MMACE8] ⇐ MONO PATTERN 0                              ; 1st 32 bits of mono pattern
ES:[MMACEC] ⇐ MONO PATTERN 0                              ; 2nd 32 bits of mono pattern
ES:[MMACF0] ⇐ DATA1 (7-0)                                 ; 8-bit pattern backgnd color index
ES:[MMACF4] ⇐ DATA1 (7-0)                                 ; 8-bit pattern foregnd color index
ES:[MMA504] ⇐ W-1 (26-16), H (10-0)                       ; rectangle width and height
ES:[MMA508] ⇐ SRC_X (26-16), SRC_Y (10-0)                 ; source x and y start coordinates
ES:[MMA50C] ⇐ DEST_X (26-16), DEST_Y (10-0)               ; destination x and y start coord.
ES:[MMA500] ⇐ 0000 000S SSSS SSS0 0000 0001 1110 00S0     ; Command Set register
```

The following must be specified: ROP (bits 24-17), first dword offset (bits 13-12), image transfer alignment (bits 11-10), clipping enable (bit 1). Bits 4-2 will be different for other color depths.

```
COUNT (of image pixel data to transfer) = (See Note)
IMAGEDATA ⇐ RECT_DATA          ; Output data to Image Transfer addresses for COUNT dwords
```

Autoexecute On:

Writing to the Destination XY register (MMA50C) executes the command.

Note

If the source bitmap is provided by the application, then the entire Note for the previous color pixels case also applies to this mono pixel case because each line is required to be word aligned. If the source bitmap is provided by the driver, e.g., font data, the driver should byte align the data and program bits 11-10 of the Command Set register to 00b to specify byte alignment to the Engine.

15.4.4.2 Rectangle Fill

This command draws a filled rectangle on the screen. Only ROPs that do not contain a source can be used. If the ROP contains a pattern, the pattern specification will be ignored. Instead, the pattern value is forced to a 1 by the hardware, selecting the pattern foreground color. ROPs specifying only the destination (screen) and optionally a logical operation (e.g., NOT D) can be used. In this case, the rectangle color will depend only on the current screen color. For this example, assume the height and width (in pixels) of the rectangle being drawn are H and W. The screen color depth is assumed to be 8 bits/pixel.

Autoexecute Off:

```
ES:[MMA4F4] ⇐ DATA1 (7-0)                                  ; 8-bit pattern foregnd color index
ES:[MMA504] ⇐ W-1 (26-16), H (10-0)                        ; rectangle width and height
ES:[MMA50C] ⇐ DEST_X (26-16), DEST_Y (10-0)                ; destination x and y start coord.
ES:[MMA500] ⇐ 0001 000S SSSS SSS0 0000 0001 0010 00S0      ; Command Set register
```

The following must be specified: ROP (bits 24-17), clipping enable (bit 1). Bits 4-2 will be different for other color depths. Bit 8 must be set to 1 to specify a mono pattern.

Autoexecute On:

Writing to the Destination XY register (MMA50C) executes the command.

15.4.4.3 2D Line Draw

This command draws a two-dimensional line on the screen. Only ROPs that do not contain a source can be used. If the ROP contains a pattern, the pattern specification will be ignored. Instead, the pattern value is forced to a 1 by the hardware, selecting the pattern foreground color. ROPs specifying only the destination (screen) and optionally a logical operation (e.g., NOT D) can be used. In this case, the line color will depend only on the current screen color. Assume x1,y1 are the starting coordinates of the requested line and x2,y2 are the ending coordinates. x1 and x2 are pixel coordinates, with 0 being the x coordinate of the first (leftmost) pixel on each line. y1 and y2 are line coordinates, with 0 being the coordinate of the first (topmost) line.

The S3d Engine draws 2D lines from the bottom up, regardless of the requested drawing direction. Figure 15-3 shows four cases of requested lines (shown by the arrows on the grids). In Case 1, the requested drawing direction is the same as is used by the S3d Engine, so the x1,y1 coordinates are used to determine the starting coordinates (X_{START}, Y_{START}). In Case 2, the line will be drawn by the S3d Engine exactly reversed from that requested, so x2,y2 are used to determine the starting coordinates. In these and the other two cases, the small arrows outside the grid point to the starting coordinates used by the S3d Engine. The programmer must always use the end with the largest y value as the starting point.

Another complexity is illustrated by Case 1. If the line is X MAJOR (i.e., for a given movement along the line, the x value increases faster than the y value), the starting x value must be adjusted to the point indicated by the intersection of the dashed lines. This is a 1/2 pixel (x direction) extension from the first pixel to be drawn. For Y MAJOR lines (Case 4), this adjustment is not required.

The parameters required to draw a line must be calculated by software and programmed into the appropriate registers. The first values that must be calculated are:

ΔX = x2 - x1 or x1 - x2
ΔY = y2 - y1 or y1 - y2

The important point is that if x2 - x1 is used for ΔX, then y2 - y1 must be used for ΔY and vice versa.

The parameters required are:

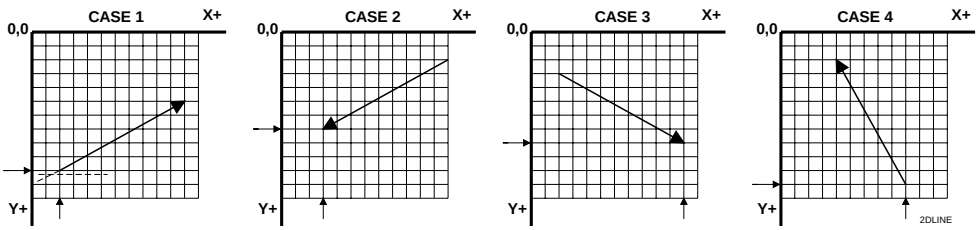


Figure 15-3. 2D Line Drawing Cases

X DELTA = - (ΔX << 20)/ΔY (integer divide)

This is value is programmed in MMA970 with bit 31 as the sign bit (0 = positive)

X START = (x_{START} << 20) + (X DELTA/2) for X MAJOR lines and positive X DELTA
X START = (x_{START} << 20) + (X DELTA/2) + ((1 << 20) - 1) for X MAJOR lines and negative X DELTA
X START = (x_{START} << 20) for Y MAJOR lines

This value is programmed in MMA974 with bits 31 and 30 as sign bits. The preceding discussion describes how to determine x_{START}.

Y START = y_{START}

This value is programmed in MMA978_10-0. It is the y value of the first scan line and is always the largest requested y.

Y COUNT = [abs (y2 -y1)] + 1

This value is programmed in MMA97C_10-0. It is the number of scanlines to draw.

The horizontal drawing direction is specified in MMA97C_31 (0 = right to left; 1 = left to right)

The final parameters to be specified are used primarily for the case where the programmer is drawing a polyline (connected line segments) and specifies "last pixel not drawn" for one segment. This is done so that the last pixel of one segment is not drawn a second time as the first pixel of the next segment. The parameters are:

END1 = x coordinate for the last pixel to be drawn for the line (MMA96C_15-0)
END0 = x coordinate for the first pixel to be drawn for the line (MMA96C_31-0)

The both cases, the 5 most significant bits are sign bits and must be 0's to indicate a positive value.

The complication here is again that the S3d Engine drawing direction may not be the same as the requested direction. In Case 1 of Figure 15-3, the two directions are the same. If "last pixel off" is specified, then END0 is programmed with the x1 (requested starting x) value and END1 with x2 -1 (one

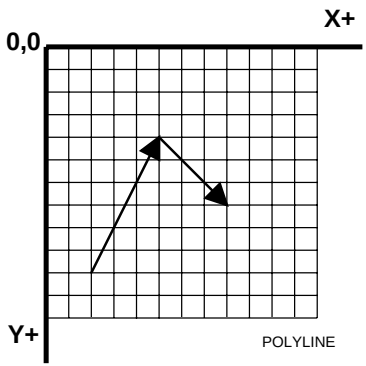


Figure 15-4. Polyline Drawing Example

less than the requested ending x value to stop the line one pixel short). In Case 2, the directions are opposite. END0 is programmed with x2 +1 and END1 with x1. Thus, the S3d Engine (which starts at the requested ending x position so it can draw upward) skips the first pixel and draws the last to accommodate the reversed drawing direction. In a similar fashion, is is easy to see that for Case 3, END0 is x2 - 1 and END1 is x1. For Case 4, END0 is x1 and END1 is x2 +1.

If "last pixel off" is not requested, the END0 and END1 values are the same as described above except that 1 is not added or subtracted as appropriate. Thus, the full x values of both ends of the line are specified. This allows a horizontal line to be drawn. Normally, the X DELTA value for a horizontal line would be infinity ($\Delta Y = 0$). For this case, the programmer can specify an X DELTA of 0 and the S3d engine will use the endpoint parameters to draw the correct line.

The following programming example is for a polyline as shown in Figure 15-4. The first requested segment goes up to the right with the last pixel not drawn. The second segment goes down to the right with all pixels drawn. This first segment must be drawn first since it has the largest y value. It is drawn as described for Case 1 in Figure 15-3 except the line is X MAJOR. The second line segment is drawn as described for Case 3. This line is neither X MAJOR or Y MAJOR, so the Y MAJOR assumption should be used because it is simpler to calculate X START. Autoexecute is used so that the Command Set register does not need to be re-programmed.

```
                                                    ; 1st line segment
ES:[MMA96C] ⇐ END0 (31-16), END1 (15-0)             ; last pixel off for END1
ES:[MMA970] ⇐ X DELTA                               ; x direction gradient
ES:[MMA974] ⇐ X START                               ; starting x coord. for S3d Engine
ES:[MMA978] ⇐ Y START (10-0)                        ; starting y coord. for S3d Engine
ES:[MMA900] ⇐ 0001 100S SSSS SSS0 0000 0000 0010 00S1  ; Command Set (autoexecute)
ES:[MMA97C] ⇐ DIR (31), Y COUNT (10-0)              ; draw dir and # of scanlines
                                                    ; 2nd line segment
ES:[MMA96C] ⇐ END0 (31-16), END1 (15-0)             ; all pixels drawn
ES:[MMA970] ⇐ X DELTA                               ; x direction gradient
ES:[MMA974] ⇐ X START                               ; starting x coord. for S3d Engine
ES:[MMA978] ⇐ Y START (10-0)                        ; starting y coord. for S3d Engine
ES:[MMA97C] ⇐ DIR (31), Y COUNT (10-0)              ; draw dir and # of scanlines
```

Note that with autoexecute on (bit 0 of the Command Set register set to 1), a line is drawn every time MMA97C is programmed. Also note that the Command Set register has a unique address for each command type, e.g., it is at offset A900 for 2D lines while it is at A500 for BitBLTs and rectangle fills. Only the ROP (bits 24-17) and clipping (bit 1) are optionally specified for line draws.

To draw a disconnected line after drawing a polyline, autoexecute must first be turned off. This is done by writing to the Command Set register with bit 0 cleared to 0 and the command (bits 30-27) specified as 1111b (NOP).

15.4.4.4 2D Polygon Fill

This command is used to generate a filled polygon. Any number of edges can be drawn, but the shape must be such that any horizontal line must intersect the polygon edges in no more than two places. The exception is that any edge can be horizontal. Only ROPs that do not contain a source can be used. If the ROP contains a pattern, the pattern specification will be taken from the appropriate color or mono pattern registers. ROPs specifying only the destination (screen) and optionally a logical operation (e.g., NOT D) can be used. In this case, the pixel color will depend only on the current screen color for the destination pixel.

For polygon fills, the end points of each edge segment are not explicitly specified and cannot be optionally drawn or not drawn. Drawing of the overlapping pixels is handled automatically. Also, instead of specifying the direction of line drawing, the edge or edges to be updated are specified via bits 28 and 29 of MMAD7C. Otherwise, the parameters for each line are calculated exactly as for 2D lines.

$\Delta X = x2 - x1$ or $x1 - x2$
$\Delta Y = y2 - y1$ or $y1 - y2$

The important point is that if x2 - x1 is used for ΔX, then y2 - y1 must be used for ΔY and vice versa.

The parameters required are:

X DELTA = - (ΔX << 20)/ΔY (integer divide) - right and left edges

These values are programmed in MMAD68 and MMAD70 with bit 31 as the sign bit (0 = positive)

X START = (x_{START} << 20) + (X DELTA/2) + (1 << 19) for X MAJOR lines - right and left edges
X START = (x_{START} << 20) + (1 << 19) for Y MAJOR lines - right and left edges

These values are programmed in MMAD6C and MMAD74 with bits 31 and 30 as sign bits. The line draw discussion describes how to determine x_{START}.

Y START = y_{START}

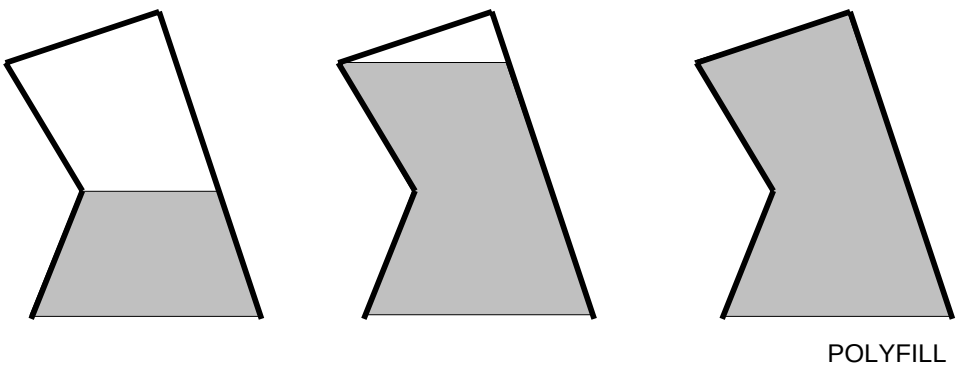


Figure 15-5. Polygon Fill Example

This value is programmed in MMA978_10-0. It is the y value of the first scan line and is always the largest requested y.

Y COUNT = [abs (y2 -y1)] + 1

This value is programmed in MMAD78_10-0. It is the number of scanlines to draw for each edge segment.

The S3d Engine draws polygons from the bottom up as shown in the example in Figure 15-5. In the first iteration, the programmer specifies line parameters for the left and right edges and specifies that they both be updated. The first iteration also specifies the number of scan lines up to the first vertex, which is on the left edge in this example. This results in the trapezoid shown in the leftmost example. The second iteration only specifies the second segment of the left edge, resulting in the middle example. Since the right edge does not change slope, it should not be re-specified or updated (MMAD7C_28 = 0). This speeds the drawing by eliminating the need for a recalculation for that edge. The third iteration draws the third segment of the left edge, which joins the right edge to complete the polygon as shown by the right hand example. Again, the right edge should not be re-specified or updated.

As with the bottom edge shown in the example, if the top edge is a horizontal line, that line does not have to be drawn to close the polygon.

```
                                                    ; 1st iteration
ES:[MMAD68] ⇐ RIGHT EDGE X DELTA                    ; right edge x direction gradient
ES:[MMAD6C] ⇐ RIGHT EDGE X START                    ; right edge starting x coord.
ES:[MMAD70] ⇐ LEFT EDGE X DELTA                     ; left edge x direction gradient
ES:[MMAD74] ⇐ LEFT EDGE X START                     ; left edge starting x coord.
ES:[MMAD78] ⇐ Y START (10-0)                        ; bottommost y value
ES:[MMAD00] ⇐ 0010 100S SSSS SSS0 0000 0000 0010 00S1   ; Command Set (autoexecute)
ES:[MMAD7C] ⇐ Update Lft (29), Update Rgt (28), Y COUNT (10-0) ; update edge and # of scanlines
                                                    ; 2nd iteration
ES:[MMAD70] ⇐ LEFT EDGE X DELTA                     ; left edge x direction gradient
ES:[MMAD74] ⇐ LEFT EDGE X START                     ; left edge starting x coord.
ES:[MMAD7C] ⇐ Update Lft (29), Update Rgt (28), Y COUNT (10-0) ; update edge(s) and # of scanli-
nes
                                                    ; 3rd iteration
ES:[MMAD70] ⇐ LEFT EDGE X DELTA                     ; left edge x direction gradient
ES:[MMAD74] ⇐ LEFT EDGE X START                     ; left edge starting x coord.
ES:[MMAD7C] ⇐ Update Lft (29), Update Rgt (28), Y COUNT (10-0) ; update edge and # of scanlines
```

Note that with autoexecute on (bit 0 of the Command Set register set to 1), a trapezoid fill is executed every time MMAD7C is programmed. Also note that the Command Set register has a unique address for each command type, e.g., it is at offset AD00 for 2D polygon fills while it is at A500 for BitBLTs and rectangle fills and A900 for 2D lines. Only the ROP (bits 24-17) and clipping (bit 1) are optionally specified for polygon fills.

15.4.5 3D Graphics Drawing

The S3d Engine accelerates the drawing of 3D lines and triangles. Texturing of 3D triangles and fogging and alpha blending of both 3D lines and 3D triangles is also supported. This section describes the basic 3D drawing capabilities and the register values required to generate the desired image. Programming code is quite complex for 3D operations and will be provided by S3 to customers desiring to create custom drivers.

15.4.5.1 3D Line Drawing

3D line drawing is very similar to 2D line drawing except:

- There is a third (Z) dimension, with increasing values going away from the viewer (into the screen). Like the X value, this is specified in fractional coordinates. (The Y value is always an integer number of scan lines.) The registers associated with this dimension are 3dZ and 3ZStart and are used only when Z-buffering is desired.
- There are 4 color coordinates for the start of the line and associated color deltas. The color values are Alpha (transparency/opacity factor), Red, Green and Blue. These are all expressed as fractional values. The registers associated with these colors are 3dGdY_dBdY and 3dAdY_dRdY (deltas) and 3GS_BS and 3AS_RS (starts).

15.4.5.2 3D Triangle Drawing

Figure 15-6 represents a typical triangle drawn into the frame buffer. The grid represents pixel coordinates, i.e., each intersection is the location of one pixel. The origin of the grid is at the top left (0,0), with the X dimension increasing to the right and the Y dimension increasing downward. The specified triangle does not have to start or end on a pixel coordinate, as illustrated in the figure.

Vertices 0 through 2 of the triangle to be drawn are numbered by decreasing Y value, i.e., from bottom to top. The triangle is always rendered from bottom to top, starting at the first scan line at or above the starting (bottom) vertex and ending at the last scan line at or below the ending (top) vertex. The location of the 02 side (largest Y dimension) determines the horizontal rendering direction. For a triangle as shown in Figure 15-6, with the 02 side on the left, rendering must be done from left to right. This is specified by setting bit 31 of MMB57C to 1. If the triangle in Figure 15-6 is flipped horizontally so the 02 side is on the right, the rendering direction must be specified as from right to left. This is done by clearing bit 31 of MMB57C to 0.

As many as 43 registers may be required to completely specify the rendering of one 3D triangle with texturing applied. These registers are described in Section 19. Figure 15-6 helps to explain the relevance of most of these registers.

The following registers are associated with point A.

Spatial Dimensions (Point A)	Color Dimensions (Point A)	Texture Dimensions (Point A)
TXStart02 TYStart TZS02	TGS_BS TAS_RS	TDS TUS TVS TWS

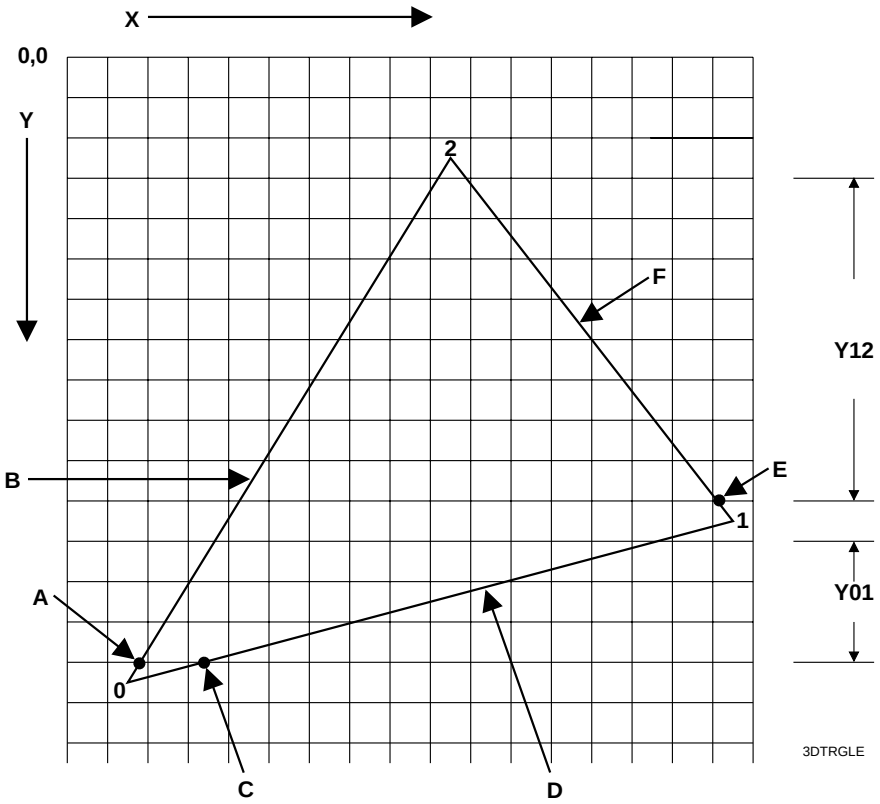


Figure 15-6. 3D Triangle Example

The following registers are associated with the Y axis and side 02. Note that the Y component of side 02 (B in Figure 15-6), always determines the number of scan lines required to render the triangle.

Spatial Dimensions (Y axis)	Color Dimensions (Y axis)	Texture Dimensions (Y axis)
TdXdY02 TdZdY TY01_Y12	TdGdY_dBdY TdAdY_dRdY	TdDdY TdUdY TdVdY TdWdY

The TXEnd01 register is associated with point C in Figure 15-6.

The following registers are associated with the X axis and side 01. Note that the X component of side 01 (D in Figure 15-6), is always the maximum width of the rendered triangle.

Spatial Dimensions (X axis)	Color Dimensions (X axis)	Texture Dimensions (X axis)
TdXdY01 TdZdX	TdGdX_dBdX TdAdX_dRdX	TdDdX TdUdX TdVdX TdWdX

The TXEnd12 register is associated with point E in Figure 15-6.

The TdXdY12 register is associated with side 12 (F in Figure 15-6).

The TbU and TbV registers contain the common offset values for the U and V texture dimensions, i.e., these values are added to all U and V specifications.

Triangles can be drawn with perspective correction (bits 30-27 of the Command Set register = 0101 or 0110). Perspective correction uses the W parameters. In addition, the U and V parameters have different bit codings when perspective correction is specified than when it is not. These are explained in the register descriptions. Using automatic perspective correction will normally cause some decrease in performance, but can in some circumstances provide dramatic increases in picture quality.

15.4.6 Z-Buffering

Z-buffering allows the programmer to eliminate rendering of hidden lines and surfaces. It is enabled when bits 25-24 of the Command Set register are 00b and bits 22-20 of the Command Set register are not 000b. Use of z-buffering requires that space be allocated in video memory for the z-buffer. The starting location is specified in the Z_BASE register. For each graphics pixel, the z-buffer contains a corresponding 16 bits of depth information. Bits 22-20 of the Command Set register specify the relational operator used to compare the z value of the source pixel with its corresponding z-buffer value, as follow:

000 = Z compare never passes
001 = Pass if Zs > Zzb
010 = Pass if Zs = Zzb
011 = Pass if Zs ≥ Zzb
100 = Pass if Zs < Zzb
101 = Pass if Zs ≠ Zzb
110 = Pass if Zs ≤ Zzb
111 = Z compare always passes

For example, a setting of 110 means that the source pixel will replace the current pixel in video memory only if its source z value is less than the corresponding z-buffer value. This is the normal comparison, as it allows the pixel closer to the viewer to be drawn. If bit 23 of the Command Set register is set to 1, the source pixel z value will replace the current z-buffer value. If bit 23 of the Command Set register is cleared to 0, the z-buffer value remains unchanged.

The z-buffer comparison occurs before any of the pixel coloring operations described below. If the z comparison fails, no further coloring operations will be done on that pixel. Similarly, if the operator is set to never pass, z-buffering is effectively disabled. This can improve performance.

15.4.7 MUX Buffering

Z-buffering requires 16 bits of video memory storage for each displayable pixel. If insufficient memory is available, MUX buffering may allow z-buffering to be performed. With MUX buffering, the active frame buffer area (draw buffer) is alternately programmed with z-buffer values and pixel colors. This requires that all the primitives (lines and triangles) of the scene be rendered twice, which decreases performance. Otherwise, MUX buffering produces the effects as normal z-buffering.

MUX buffering can only be used when the destination format is 16 bits/pixel and no alpha blending is to be performed (bit 19 of the Command Set register = 0). When the destination format is 16 bits/pixel, bit 15 = 1 indicates the word contains a z value and bit 15 = 0 indicates the word contains an RGB555 value.

With MUX buffering, double buffering should be used so that the z-buffering can be done in the inactive (back) buffer. See the Streams Processor section for an explanation of double buffering. Z-buffering is enabled as explained in the previous section except that bit 23 of the Command Set register must be set to 1 so that the source pixel z value will replace the current z-buffer value. As a final setup step, the entire buffer must be written with either a solid color or a prerendered bitmap. This sets the z bit of each word to 0, indicating that colors are stored.

On the first pass, bits 25-24 of the Command Set register are programmed to 01b to specify the z-buffer pass. The S3d Engine interpolates only the z values of the the source primitive (line or triangle). For each source pixel, if the corresponding destination pixel is a color (bit 15 = 0), the source z value replaces the destination color. For the first primitive to be drawn for the scene, the source pixels (z values) will replace all the corresponding destination pixels (colors) because of the initialization to colors. For subsequent primitives for the scene, the source pixel may or may not replace the destination pixel. It will always replace it if the destination is a color, but if the destination is a z-value, it will only replace it if the z comparison passes. At the end of this pass, all pixels corresponding to primitives are set to z values. All other pixels retain the initialization color values.

For the second pass, bits 25-24 of the Command Set register are programmed to 10b to specify the draw buffer pass. The S3d Engine again interpolates the z values for all source primitives. If the destination pixel is a color, that pixel color is left unchanged. If the destination pixel is a z value, the source z value is compared with the destination z value. If they are equal, the source color is computed and that color value replaces the destination z value. At the end of this pass, all pixels in the buffer contain color values. The buffer is then switched to the front (active) and is used for the next screen refresh.

15.4.8 3D Pixel Color Generation

Pixel color generation for 3D drawing occurs in a series of steps as depicted in Figure 15-7. The first of these, calculate the source pixel color, has been explained in the 3D line and triangle drawing sections above. The remaining steps are:

1. Filter - If texturing is enabled for a 3D triangle, two, four or eight texels (texture pixel) from the texture map can be filtered (interpolated) to generate a texture color to be mixed with the source color in step 3 or a code to be used in the next step.
2. Generate - For certain applications, textures can be stored in a compact colorless mode (Blend4). This step generates a texture color based on the compact coding, which may or may not be the output of filtering from the previous step. This color is used in the next step.

3. Light - If a lit texture triangle is specified, the source pixel color is mixed with the texel color to generate a color which can optionally be fogged or alpha blended.
4. Fog - Also called depth cueing. As shown in Figure 15-7, the input can either be the source pixel color or the result of the filter/generate steps.
5. Alpha Blend - The source pixel color or the output of the fogging step (which may be disabled) is blended with the destination pixel color in video memory. This can produce a transparency effect.

Each of these steps is explained in more detail in the following sections.

15.4.8.1 Texture Filtering

Textures are stored in off-screen video memory at a location specified in MMB4EC. The integer components of the U and V parameters generate the memory addresses for each texture element, which is called a texel. The fractional part of the U and V parameters are used in the filter stage for interpolation between texel colors. The texture color format is specified in bits 7-5 of the Command Set register and can be one of the following:

000 = 32 bits/pixel (ARGB8888)
001 = 16 bits/pixel (ARGB4444)
010 = 16 bits/pixel (ARGB1555)
011 = 8 bits/pixel (Alpha4, Blend4)
100 = 4 bits/pixel (Blend4, low nibble)
101 = 4 bits/pixel (Blend4, high nibble)
110 = 8 bits/pixel (palettized)
111 = YU/YV (16 bits/pixel equivalent)

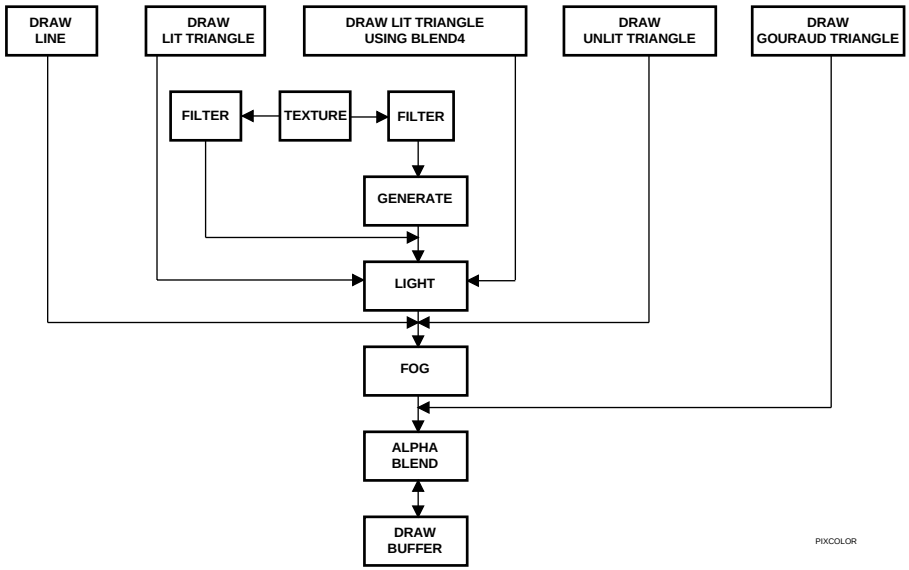


Figure 15-7. Pixel Coloring

The texture can be a single rectangular pattern or a MIPmap. A MIPmap contains multiple versions of the same texture, each at successively lower resolutions (1/2, 1/4, 1/8, etc.). The size of the largest MIPmap level (level 0) must be specified via bits 11-8 of the Command Set register. The integer part of the D parameter points to the MIPmap level to be used for the texture. The fractional part of the D parameter is used for filtering of colors between MIPmap levels.

A variety of filter modes are provided via bits 14-12 of the Command Set register, as follows:

000 = M1TPP (MIP_NEAREST)
001 = M2TPP (LINEAR_MIP_NEAREST)
010 = M4TPP (MIP_LINEAR)
011 = M8TPP (LINEAR_MIP_LINEAR)
100 = 1TPP (NEAREST)
101 = Fast Bilinear
110 = 4TPP (LINEAR)
110 = Reserved

Modes starting with M are MIPmapped. Those without have a single texture level. XTPP means X texels are interpolated per source pixel. Figure 15-8 demonstrates the effect of the 011 setting (M8TPP). The U,V and D parameters point to the texture map location indicated by the black dot at F. To generate the color for this location, the four nearest pixels in MIPmap level D (1 - 4) are interpolated to generate the color indicated by the top medium gray dot (I1). The four nearest pixels in MIPmap level D + 1 (5 - 8) are interpolated to generate the color indicated by the bottom medium gray dot (I2). The colors at I1 and I2 are then interpolated to produce the final color at F.

If M1TPP or 1TPP is selected, the texel nearest to the programmed texture location is chosen to provide the texture color. For M2TPP, the color is interpolated between the nearest texels from 2 MIPmap levels (e.g., texels 1 and 5 in Figure 15-8). For M4TPP or 4TPP, texels 1, 2 , 3 and 4 are interpolated. For V2TPP, which is used only for YUV data, texels 1 and 3 are interpolated.

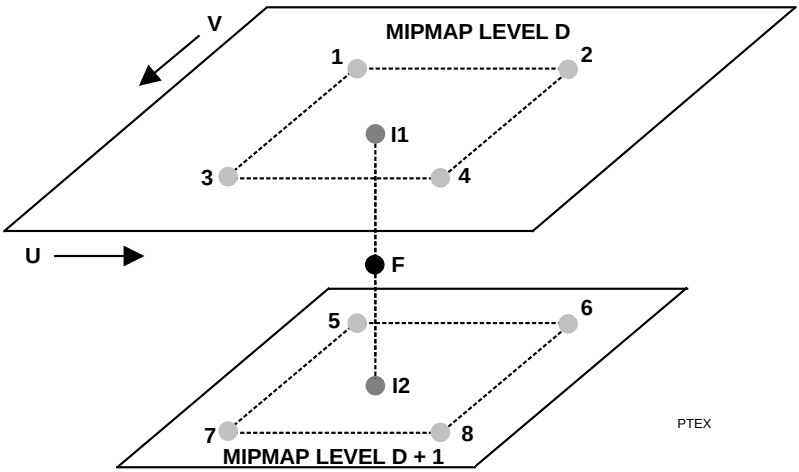


Figure 15-8. Texture Filtering

Filtering of 8 bits/pixel palettized data produces uncertain results. Palettized texel colors can be used if the filter mode is M1TPP or 1TPP (only one texel is used to generate the color) and the texture blending mode (lighting) is specified as decal. This means the texel color replaces the source pixel color (no mixing). Because the color is now palettized, it cannot be texture lit, fogged or alpha blended.

15.4.8.2 Generation

ViRGE/MX provides several compact texture storage modes, called Blend4 (high and low nibble) and Alpha4/Blend4. Blend4 uses 4 bits to define the color for each texel. These bits can be in either the high or low nibble of each byte, allowing the programmer to locate texels from two different textures in a single byte. Alpha4/Blend4 has 4 bits of Alpha coding and 4 bits of RGB color coding in each byte.

Blend4 is useful for textures with a narrow range of colors, such as grass. The 4-bit value is an interpolation factor between two RGB colors defined in the Color 0 (MMB4F8) and Color1 (MMB4FC) registers.

Alpha4/Blend4 is useful for textures with a limited range of colors and transparency, such as a cloudy sky. In this case, there are a few shades of blue-white, with whiter clouds being more opaque than bluer sky. Alpha blending is explained below.

Generation of colors for Blend4 modes occurs after the filter phase. Therefore it is possible to filter multiple Blend4 texels to produce a composite color interpolation factor to be used in the generate phase. The results of this might be hard to predict. The filter phase can be bypassed by selecting a 1TPP filter mode.

15.4.8.3 Lighting

Lighting is the blending of the texel color with the source pixel color. As seen in Figure 15-7, it is used only when a lit triangle is specified in bits 30-27 of the Command Set register. Bits 16-15 of the Command Set register specify the blending modes as follows:

00 = Complex reflection
01 = Modulate
10 = Decal
11 = Reserved

Complex reflection adds the (normalized, 0 = black and 1 = white) texel and pixel colors, with a maximum value of 1. This lightens the pixel.

Modulate multiplies the normalized color values. This results in a smaller value (darker pixel). The programmer may need to compensate for this darkening effect.

Decal uses the texture alpha value to interpolate between source color and texture color. The equation used is Cout = Atex * Ctex + (1-Atex) * Cpix.

If the texture map is smaller than the area to be textured, texture wrapping can be turned on via bit 26 of the Command Set register. This allows the texture to be tiled across the scene. If texture wrapping is disabled and and the texture map is smaller than the area to be textured, the texel color is taken from the Texture Border Color register (MMB4F0) for all pixels beyond the texture.

15.4.8.4 Fogging

Fogging is enabled via bit 17 of the Command Set register. This operation uses the pixel's alpha value to interpolate between the pixel color at this stage of the coloring process (see Figure 15-7) and a fog color specified in MMB(0/4)F4. If the alpha value corresponds to the distance from the viewer, this is called depth cueing. If fogging is being done, source alpha cannot be specified for alpha blending (i.e., bits 19-18 of the Command set register cannot be 11b).

15.4.8.5 Alpha Blending

Alpha blending blends the pixel color at this stage of coloring (see Figure 15-7) with the color of the corresponding pixel in the draw buffer. It is enabled via bits 19-18 of the Command Set register. If these bits are 10b, the texture alpha is used for the interpolation factor. The texture alpha is actually the alpha for the pixel at this stage of the coloring and not a texel alpha. If bits 19-18 are 11b, the source alpha is used for the interpolation factor. This is the original pixel alpha before texturing.

Alpha blending is used for transparency effects. The smaller the value of alpha, the more the destination color will dominate the final color (or higher transparency). To be effective with Z-buffering enabled, all opaque objects must be drawn first. Then all transparent objects are drawn with z-update disabled (MMB500_23 = 0). To be effective with Z-buffering disabled, objects must be drawn back to front.

15.4.9 3D Enhancements

The S3d Engine used in ViRGE/MX is an extended version of the S3 ViRGE™ S3d Engine. Most of the enhancements provide greater performance and are software transparent. There are also new modes available that require software modifications for use.

MMB500_14-12

101 = Fast Bilinear mode

This new filtering mode replaces the unused V2tpp mode in the original ViRGE engine. This provides an approximate 3x speed enhancement for perspective corrected point sampled texturing.

ViRGE/MX will power on in ViRGE-compatible mode (MMB508_31 = 0). When MMB508_31 is set to 1, Extended S3d mode is enabled. The only register incompatibilities with ViRGE mode are:

MMB508_31-29

0xx = ViRGE compatible mode
100 = Extended S3d mode without D change
101 = Extended S3d mode; L0 - (fastlog2 D)
110 = Extended S3d mode; L0 - (2 * fastlog2 D)
111 = Extended S3d mode; L0 - (1.5 * fastlog2 D)

MMB504_31-22

Value = L0 constant for the log D calculation

Triangle commands without perspective are no longer supported (MMB500_30-27 = 0001b and 0010b are now reserved), wrap disable (MMB500_26 = 0) is not supported and the border color register

(MMB4F0) becomes meaningless. In addition, the bit formats for MMB504, MMB50C, MMB51C, MMB520, MMB528, MMB52C, MMB534, MMB538 are changed as described in Section 19.

15.5 PROGRAMMABLE HARDWARE CURSOR

A programmable cursor is supported. The cursor size is 64 pixels wide by 64 pixels high, with the cursor pattern stored in an off-screen area of display memory. Two monochrome images 64 bits wide by 64 bits high (512 bytes per image) define the cursor shape. The first bit image is an AND mask and the second bit image is an XOR mask. The following is the truth table for the cursor display logic.

AND Bit	XOR Bit	Displayed (Microsoft Windows)
0	0	Cursor Background Color
0	1	Cursor Foreground Color
1	0	Current Screen Pixel
1	1	NOT Current Screen Pixel

The hardware cursor color is taken from the Hardware Graphics Cursor Foreground Stack (CR4A) and the Hardware Graphics Cursor Background Stack (CR4B) registers. Each of these is a stack of three 8-bit registers. The stack pointers are reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). The color value is then programmed by consecutive writes (low byte, second byte, third byte) to the appropriate (foreground or background) register.

Enabling/Disabling the Cursor

The hardware cursor is disabled when a VGA-compatible mode is in use. It can be enabled or disabled when in Enhanced mode (bit 0 of 4AE8H = 1), as follows.

```
CR39 ⇐ A0H          ; Unlock System Control registers
CR45_0 ⇐ 1          ; Enable hardware cursor
CR45_0 ⇐ 0          ; Disable hardware cursor
CR39 ⇐ 00H          ; Lock System Control registers
```

Positioning the Cursor

The cursor can be positioned at any point on the display, with the X,Y coordinates ranging from 0 to 2047. This enables the full cursor images to be displayed on the screen and partial cursor images to be displayed at the right edge and the bottom edge of the screen. The cursor offset OX,OY has to be set to 0,0 for a 1024x768 resolution. If X is > (1024 – 64) or Y is > (768 – 64), then a partial cursor is visible at the right edge or top edge of the screen respectively. Note that if Y ≥ 768 then the cursor is not visible; it is residing in the off-screen area.

A partial cursor image can be displayed at the left edge or the top edge of the screen. To enable partial cursor display at the top edge of the screen, Y is set to 0 and the Y offset register is set to OY (range from 0 to 63). This displays the bottom 64–OY rows of the cursor image at the currently set X position and the top edge of the screen. Similarly, a partial cursor can be displayed at the left edge of the screen by setting X to 0 and the X offset register to OX (range from 0 to 63). This displays the right 64–OX columns of the cursor image at the currently set X and the left edge of the screen. The following pseudocode illustrates cursor positioning.

```
CR39 ⇐ A0H                          ; Unlock System Control registers
CR46_10-8 ⇐ MS 3 bits of X cursor position
```

CR47_7-0 ⇐ LS 8 bits of X cursor position
CR49_7-0 ⇐ LS 8 bits of Y cursor position
CR4E_5-0 ⇐ Cursor Offset X position
CR4F_5-0 ⇐ Cursor Offset Y position
CR48_10-8 ⇐ MS 3 bits of Y cursor position
CR39 ⇐ 00H ; Lock System Control registers

The cursor position is updated by the hardware once each frame. Therefore, the programmer should ensure that the position is re-programmed no more than once for each vertical sync period.

Programming the Cursor Shape

The AND and the XOR cursor image bitmaps are 512 bytes each. These bitmaps are word interleaved in a contiguous area of display memory, i.e., AND word 0, XOR word 0, AND word 1, XOR word 1 ... AND word 255, XOR word 255. The starting location must be on a 1024-byte boundary. This location is programmed into the Hardware Graphics Cursor Start Address registers (CR4C and CR4D) as follows:

CR39 ⇐ A0H ; Unlock System Control registers
CR4C_11-8 ⇐ MS 4 bits of the cursor storage start 1024-byte segment.
CR4D ⇐ LS 8 bits of the cursor storage start 1024-byte segment
CR39 ⇐ 0 ; Lock System Control registers

The value programmed is the 1024-byte segment of display memory at which the beginning of the hardware cursor bit pattern is located. The cursor pattern is programmed (using linear addressing) at FF800H offset from the base address of the frame buffer.

Cursor Destination

If in DuoView mode, select the cursor controller source. SR31_7 = 0 selects Controller 1; SR31_7 = 1 selects Controller 2. This determines on which screen the cursor will appear.

Underscanning

Underscanning for TV out display is enabled for the hardware cursor by setting SR7D_2 to 1. This enables appropriate deletion of vertical lines from the cursor, but does not adjust for the cursor location shift. This must be done by software.

Note

If the cursor is not 64 bits by 64 bits, the given images should be padded to make the cursor image 64 bits by 64 bits. The padded area should be made transparent by padding the extra AND mask bits with '1's and the extra XOR bits by '0's.

15.6 PROGRAMMABLE HARDWARE ICON

ViRGE/MX provides a programmable hardware icon that is displayable in all modes, including VGA text and graphics modes. Only the hardware cursor (available only in Enhanced modes) has precedence over the hardware icon for overlaying on the text/graphics/video.

The setup for using a hardware icon involves two steps.

1. Multiple icons are defined in contiguous memory. Each icon is defined in memory as 64 consecutive lines of pixels with 64 pixels per line and 2 bits/pixel, thus requiring 1 KByte of memory per icon. The two bits per pixel are stored in memory in the same manner as the AND and XOR masks for the hardware cursor. That is, one word of bit 1 is stored, then one word of bit 2, a second word of bit 1, a second word of bit 2, etc. Corresponding bit 1's and bit 2's are used to select the icon pixel colors.
2. Four icon colors are programmed in SR49. This address contains a stack of of twelve 8-bit registers that can be written sequentially with automatic address indexing. This allows rapid specification of four 24-bit colors (Color0 to Color3).

To use an icon, do the following:

1. Enable the hardware icon by setting SR48_0 to 1.
2. Specify the starting address in the frame buffer for the desired icon via SR48_7-4 and SR4E_7-0.
3. Specify the color of each pixel. The programmer first selects a color mode via SR48_1 as follows:
   0 = 4 opaque colors
   1 = 3 opaque colors and 1 transparent color

   When this bit is cleared to 0, the two bits programmed for each pixel in the icon memory are interpreted as follows:
   00 = Color0
   01 = Color1
   10 = Color2
   11 = Color3

   When this bit is set to 1, the two bits programmed for each pixel in the icon memory are interpreted as follows:
   00 = Color0
   01 = Color1
   10 = Color2
   11 = Transparent (the current frame buffer pixel is not overwritten)
4. Specify the final size of the icon. If SR48_2 = 0, the horizontal size is 64 pixels. If SR48_2 = 1, the horizontal size is 128 pixels. If SR48_3 = 0, the vertical size is 64 pixels. If SR48_3 = 1, the vertical size is 128 pixels. In both case, the expansion is done by pixel doubling.
5. If in DuoView mode, select the icon controller source. SR31_6 = 0 selects Controller 1; SR31_6 = 1 selects Controller 2. This determines on which screen the image will appear.
6. Program the icon location on the screen. The horizontal coordinate of the upper left hand edge of the icon is programmed in SR4A and SR4B. the vertical coordinate of the upper left hand edge of the icon is specified in SR4C and SR4D.

Underscanning for TV out display is enabled for the icon by setting SR7D_3 to 1. This enables appropriate deletion of vertical lines from the icon, but does not adjust for the icon location shift. This must be done by software.

15.7 BUS MASTER DMA

For PCI systems, ViRGE/MX provides bus master DMA capabilities. There are two independent DMA channels. One handles transfers of video data to video memory or an MPEG decoder and from video memory to system memory. The other is used to transfer command and parameter or image data to the S3d Engine.

5.7.1 Video/Graphics DMA Transfers

These transfers are enabled by setting MM8588_0 to 1. If MM8580_1 = 1, data is transferred from system memory to the LPB output FIFO. This can be compressed video data for transfer to an MPEG decoder or de-compressed software MPEG data to be written to video memory with optional decimation. See the LPB section for the appropriate register settings for each type of transfer. For either case, the starting address in system memory for the data to be transferred is programmed in MM8580_31-2 (doubleword aligned). The number of doublewords to transfer -1 is programmed in MM8584_23-2.

If MM8580_1 = 0, data is transferred from video memory to system memory. The starting address in video memory is programmed in MM8220_21-3 (quadword aligned). The line width in quadwords is programmed in MM8224_27-19 and the line stride in quadwords is programmed in MM8224_11-3. The destination starting address in system memory is programmed in MM8580_31-2 (doubleword aligned). The number of doublewords to transfer -1 is programmed in MM8584_23-2.

5.7.2 S3d Engine Command/Parameter/Image Data DMA Transfers

The type of transfer requires establishment of a locked circular buffer in system memory. MM8590_1 defines this buffer as being 4 or 64 KBytes. The base address for the buffer is programmed in MM8590_31-12 (4K) or 31-16 (64K). S3d Engine DMAs are enabled by setting MM859C_0 to 1.

The DMA write and read pointer registers (MM8594 and MM8598) are initialized to all 0's. The transfer sequence begins with the CPU writing some amount of data to the buffer. This data is derived from the parameter blocks passed to the driver by the application via the programming interface. In general, the transfer should include one or more complete command/parameter/data blocks. After this data is written to the buffer, the next offset address in the frame buffer is programmed into the DMA write pointer field (MM8594_15-0) and MM8594_16 is set to 1 to indicate that the write pointer has been updated. When the write pointer is ahead of the read pointer (MM8598_15-0), DMA transfers to the S3d Engine begin. The read pointer field is automatically updated as each doubleword transfer to the S3d Engine is made. DMA transfers will continue as long as the write pointer is ahead of the read pointer. They stop when the read pointer equals the write pointer.

Additional data can be written to the buffer at any time, starting at the current write pointer address. Wrapping of the writes when the end of the buffer is reached is handled by the programmer. Before writing additional data to the buffer, the programmer must first read the read pointer to determine how much space is available in the buffer. If this is not done, the write data could wrap and overwrite good data before it is read from the buffer.

Each update of the circular buffer must start with a doubleword header that defines what is to follow. The format of this header is:

Bit(s)	Description
15-0	Number of doublewords to transfer
29-16	Most significant 14 bits of the least significant 16 bits of the offset of the first S3d register to be programmed
30	Reserved
31	Data type (0 = register data, 1 = image data)

If image data is being transferred (a BitBLT with the CPU as the source), only bit 31 (=1) and bits 15-0 need be programmed.

This capability allows updating of multiple S3d registers in one DMA operation. For example, defining a color pattern with an 8 bits/pixel color depth requires that all registers from A100H to A13CH be programmed. Thus, bits 15-0 would be programmed with 16 (decimal). The most significant 14 bits of A100H (dropping the two low-order 0's) are programmed into bits 29-16. Bit 31 is cleared to 0.

The parameter register address ranges for some of the commands contain "holes" (no register). The programmer can either send a new header for each contiguous register sequence or program garbage in the doublewords corresponding to the holes. For example, there is a single doubleword gap between the 3AS_RS parameter register for a 3D line and the 3dZ parameter register. This is probably best handled by the "garbage" technique.

Section 16: VGA Register Descriptions

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). A question mark in an address stands for a hexadecimal value of either 'B' or 'D'. If bit 0 of the Miscellaneous Output Register (3C2H, Write) is set to 1, the address is based at 3DxH for color emulation. If this bit is reset to 0, the address is based at 3BxH for monochrome emulation. If a register or bit is noted as paired, there are two identical registers or bit at that address, with access controlled via SR26. One register or bit is used by Controller 1 and the other for Controller 2.

See Appendix A for a table listing each register in this section and its page number.

16.1 GENERAL REGISTERS

This section describes general input status and output control registers.

Miscellaneous Output Register (MISC)

Write Only Address: 3C2H
Read Only Address: 3CCH
Power-On Default: 00H

This register controls miscellaneous output signals. A hardware reset sets all bits to zero.

7	6	5	4	3	2	1	0
SYNPOL/ VERT SIZE		PGSL	= 0	CLK 1	SEL 0	ENB RAM	IOA SEL

Bit 0 IOA SEL - I/O Address Select
0 = Monochrome emulation. Address based at 3Bx
1 = Color emulation. Address based at 3Dx

Bit 1 ENB RAM - Enable CPU Display Memory Access
0 = Disable access of the display memory from the CPU
1 = Enable access of the display memory from the CPU

Bits 3–2 Clock Select - Select the Video Clock Frequency
00 = Controller 1 DCLK (either DCLK1 or DCLK2) PLL M & N parameters are taken from SR22 and SR23 unless this DCLK is also driving Controller 2, in which case the parameters are taken from SR12 and SR13 for DCLK1 or SRE and SRF for DCLK2. The default generates a value of 25.175 MHz for 640 horizontal pixels.
01 = Controller 1 DCLK (either DCLK1 or DCLK2) PLL M & N parameters are taken from SR24 and SR25 unless this DCLK is also driving Controller 2, in which case the parameters are taken from SR12 and SR13 for DCLK1 or SRE and SRF for DCLK2. The default generates a value of 28.322 MHz for 720 horizontal pixels.
10 = Reserved
11 = DCLK PLL M & N parameters are taken from SR12 and SR13 for DCLK1 and SRE and SRF for DCLK2.

The selected DCLK PLL parameter values are loaded into the PLL when bit 1 of SR15_1 is set to 1 or when SR15_5 is programmed to 1 and then 0.

Bit 4 Reserved = 0

Bit 5 PGSL -Select High 64K Page
0 = Select the low 64K page of memory
1 = Select the high 64K page of memory

Bits 7-6 SYNCPOL/VERT SIZE - Sync Polarity/Vertical Size

Bit 7	Bit 6	VSYNC Polarity	HSYNC Polarity	Vertical Size (lines)
0	0	+	+	Reserved
0	1	+	-	200 (double scanned)
1	0	-	+	350
1	1	-	-	480

+ = positive sync pulse
- = negative sync pulse

Vertical Size = vertical resolution of the graphics source

This vertical size is used when CR70_1 is set to 1 to enable graphics mode vertical expansion. During simultaneous display, SR32_2-1 control the polarity of the the VSYNC and HSYNC signals.

Feature Control Register (FCR_WT, FCR_AD)

Write Only Address: 3?AH
Read Only Address: 3CAH
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	VSSL	= 0	= 0	= 0

Bits 2–0 Reserved = 0

Bit 3 VSSL - Vertical Sync Type Select
0 = Enable normal vertical sync output to the monitor
1 = The 'vertical sync' output is the logical OR of 'vertical sync' and 'vertical active display enable' (an internal signal)

Bits 7–4 Reserved = 0

Input Status 0 Register (STATUS_0)

Read Only Address: 3C2H
Power-On Default: Undefined

This register indicates the status of the VGA adapter.

7	6	5	4	3	2	1	0
CRT INTPE	= 0	= 0	MON SENS	= 0	= 0	= 0	= 0

Bits 3–0 Reserved = 0

Bit 4 MON SENS - Monitor Sense Status
0 = The internal $\overline{\text{SENSE}}$ signal is a logical 0
1 = The internal $\overline{\text{SENSE}}$ signal is a logical 1

Bits 6–5 Reserved = 0

Bit 7 CRT INTPE - CRT Interrupt Status
0 = Vertical retrace interrupt cleared
1 = Vertical retrace interrupt pending

See Section 13.5 for an explanation of interrupt generation.

Input Status 1 Register (STATUS_1)

Read Only Address: 3?AH
Power-On Default: Undefined

This register indicates video sync timing and video wraparound.

7	6	5	4	3	2	1	0
= 0	= 0	TST-VDT 1	0	VSY	= 1	R	DTM

Bit 0 $\overline{\text{DTM}}$ - Display Mode Inactive
0 = The display is in the display mode.
1 = The display is not in the display mode. Either the horizontal or vertical retrace period is active

Bit 1 Reserved = 0

Bit 2 Reserved = 1

Bit 3 VSY - Vertical Sync Active
0 = Display is in the display mode
1 = Display is in the vertical retrace mode

Bits 5–4 TST-VDT - Video Signal Test
Video Data Feedback 1,0. These bits are feedback video signals to do read back tests. These bits are selectively connected to two of the eight color outputs of the attribute controller. Bits 5 and 4 of the color plane enable register (AR12) control the multiplexer for this video output observation.

Bits 7–6 Reserved = 0

Video Subsystem Enable Register

Write Only Address: 3C3H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	CHIP ENB

Bit 0 CHIP ENB - Chip Enable
0 = Chip disabled
1 = Chip enabled

Bits 7–1 Reserved

16.2 SEQUENCER REGISTERS

The sequencer registers are located at two-byte address spaces. These registers are accessed by first writing the data to the index register of the sequencer at I/O address 3C4H and then writing to or reading from the data register at 3C5H. A word write of both address and data at 3C4H can also be performed.

Sequencer Index Register (SEQX)

Read/Write Address: 3C4H
Power-On Default: Undefined

This register is loaded with a binary value that indexes the sequencer register for read/write data. This value is referred to as the "Index Number" of the SR register in this document. This register is also used to access the extended sequencer registers.

7	6	5	4	3	2	1	0
SEQUENCER REGISTER INDEX							

Bits 7–0 SEQUENCER REGISTER INDED
A binary value indexing the register where data is to be accessed.

Sequencer Data Register (SEQ_DATA)

Read/Write Address: 3C5H
Power-On Default: Undefined

This register is the data port for the sequencer register indexed by the Sequencer Index register (3C4H).

7	6	5	4	3	2	1	0
SEQUENCER REGISTER DATA							

Bit 7–0 SEQUENCER REGISTER DATA
Data to the sequencer register indexed by the sequencer address index.

Reset Register (RST_SYNC) (SR0)

Read/Write Address: 3C5H, Index 00H
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	SYN RST	ASY RST

Bit 0 $\overline{\text{ASY}}$ RST - Asynchronous Reset

This bit is for VGA software compatibility only. It has no function for 86CM65.

Bit 1 $\overline{\text{SYN}}$ RST - Synchronous Reset

This bit is for VGA software compatibility only. It has no function for 86CM65.

Bits 7–2 Reserved = 0

Clocking Mode Register (CLK_MODE) (SR1)

Read/Write Address: 3C5H, Index 01H
Power-On Default: 00H

This register controls the operation mode of dot clock and character clock.

7	6	5	4	3	2	1	0
= 0	= 0	SCRN OFF	SHF 4	CCLK 1/2	SHF LD	= 0	8DC

Bit 0 8DC - 8 Dot Clock Select
0 = Character clocks 9 dots wide are generated
1 = Character clocks 8 dots wide are generated

Bit 1 Reserved = 0

Bit 2 SHF LD - Load Serializers Every Second Character Clock
0 = Load the video serializer every character clock
1 = Load the video serializers every other character clock

Bit 3 CCLK 1/2 - Internal Character Clock Divided by 2
0 = Internal character clock unchanged
1 = Halve the frequency of the character clock

This bit is used for horizontal pixel doubling.

Bit 4 SHF 4 - Load Serializers Every Fourth Character Clock
0 = Load the serializers every character clock cycle
1 = Load the serializers every fourth character clock cycle

Bit 5 SCRN OFF - Screen Off
0 = Screen is turned on.
1 = Screen is turned off

This bit is effective only when CR71_1 = 0. When this bit is set, up to 3 HSYNCs may elapse before the screen is turned off. Software must be careful to allow this amount of time to pass before writing to registers that must be programmed during screen off.

Bits 7–6 Reserved = 0

Enable Write Plane Register (EN_WT_PL) (SR2)

Read/Write Address: 3C5H, Index 02H
Power-On Default: 00H

This register selects write protection or write permission for CPU write access into video memory.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	EN.WT.PL.			

Bits 3–0 EN.WT.PL - Enable Write to a Plane
0 = Disables writing into the corresponding plane
1 = Enables the CPU to write to the corresponding color plane

Bits 7–4 Reserved = 0

Character Font Select Register (CH_FONT_SL) (SR3)

Read/Write Address: 3C5H, Index 03H
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	SLA 2	SLB 2	SLA 1	SLA 0	SLB 1	SLB 0

In text modes, bit 3 of the attribute byte normally turns the foreground intensity on or off. This bit can be redefined to be a switch between two character sets. The switch is enabled when there is a difference between the value of character font select A and character font select B bits. Memory Mode (SR4) register bit 1 = 1 (extended memory) enables all bits of this function; otherwise character fonts 0 and 4 are available. 256 KBytes of video memory support 8 character sets. This register is reset to 0 asynchronously during a system reset.

Bits 4, 1–0 SLB - Select Font B
This value selects the portion of plane 2 used to generate text character fonts when bit 3 of the attribute byte is a logical 1, according to the following table:

Bits 4,1,0	Font Table Location	Bits 4, 1,0	Font Table Location
000	First 8K of plane 2	100	Second 8K of plane 2
001	Third 8K of plane 2	101	Fourth 8K of plane 2
010	Fifth 8K of plane 2	110	Sixth 8K of plane 2
011	Seventh 8K of plane 2	111	Eighth 8K of plane 2

Bits 5, 3–2 SLA - Select Font A
This value selects the portion of plane 2 used to generate text character fonts when bit 3 of attribute byte is a logical 0, according to the same table as the character font select B.

Bits 7–6 Reserved = 0

Memory Mode Control Register (MEM_MODE) (SR4)

Read/Write Address: 3C5H, Index 04H
Power-On Default: 00H

This register controls CPU memory addressing mode.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	CHN 4M	SEQ MODE	EXT MEM	= 0

Bit 0 Reserved = 0

Bit 1 EXT MEM - Extended Memory Access
0 = Memory access restricted to 16/32 KBytes
1 = Allows complete memory access to 256 KBytes. Required for VGA

Bit 2 SEQ MODE - Sequential Addressing Mode
This bit affects only CPU write data accesses into video memory. Bit 3 of this register must be 0 for this bit to be effective.
0 = Enables the odd/even addressing mode. Even addresses access planes 0 and 2. Odd addresses access planes 1 and 3
1 = Directs the system to use a sequential addressing mode

Bit 3 CHN 4M - Select Chain 4 Mode
0 = Enables odd/even mode.
1 = Chain 4 Mode. This bit selects modulo 4 addressing for CPU access to display memory. A logical 1 directs the two lower order bits of the CPU address used to select the plane in video memory to be accessed as follows:

A1	A0	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

Bits 7–4 Reserved = 0

16.3 CRT CONTROLLER REGISTERS

The CRT controller registers are located at two locations in I/O address space. These registers are accessed by first writing to the index register of the CRT controller and then accessing the data register. The index register is located at I/O address 3?4H and the CRT Controller Data register is at 3?5H. Which address is used (3BX or 3DX) depends on bit 0 of the Miscellaneous Output register at 3C2H. A word write of both address and data at 3?4H can also be performed.

CRT Controller Index Register (CRTC_ADR) (CRX)

Read/Write Address: 3?4H
Power-On Default: 00H

This register is loaded with a binary value that indexes the CRT controller register where data is to be accessed. This value is referred to as the "Index Number" of the CR register (CR00–18). This register is also used to access the extended CRTC registers.

7	6	5	4	3	2	1	0
CRTC ADDRESS							

Bits 7–0 CRTC ADDRESS - CRTC Register Index
A binary value indexing the register where data is to be accessed.

CRT Controller Data Register (CRTC_DATA) (CRT)

Read/Write Address: 3?5H
Power-On Default: Undefined

This register is the data port for the CRT controller register indexed by the CRT Controller Address register.

7	6	5	4	3	2	1	0
CRTC DATA							

Bits 7–0 CRTC DATA - CRTC Register Data
Data to the CRT controller register indexed by the CRT controller address index.

Horizontal Total Register (H_TOTAL) (CR0)

Read/Write Address: 3?5H, Index 00H
Power-On Default: Undefined Paired

This register defines the number of character clocks from HSYNC going active to the next HSYNC going active. In other words, it is the total time required for both the displayed and non-displayed portions of a single scan line. Bit 8 of this value is bit 0 of CR5D.

7	6	5	4	3	2	1	0
HORIZONTAL TOTAL							

Bits 7–0 HORIZONTAL TOTAL.
9-bit Value = (number of character clocks in one scan line) - 5. This register contains the least significant 8 bits of this value.

Horizontal Display End Register (H_D_END) (CR1)

Read/Write Address: 3?5H, Index 01H
Power-On Default: Undefined Paired

This register defines the number of character clocks for one line of the active display. Bit 8 of this value is bit 1 of CR5D. This register is locked/unlocked via CR35_6.

7	6	5	4	3	2	1	0
HORIZONTAL DISPLAY END							

Bits 7–0 HORIZONTAL DISPLAY END
9-bit Value = (number of character clocks of active display) - 1. This register contains the least significant 8 bits of this value.

Start Horizontal Blank Register (S_H_BLNK) (CR2)

Read/Write Address: 3?5H, Index 02H
Power-On Default: Undefined Paired

This register specifies the value of the character clock counter at which the $\overline{\text{BLANK}}$ signal is asserted. Bit 8 of this value is bit 2 of CR5D.

7	6	5	4	3	2	1	0
START HORIZONTAL BLANK							

Bits 7–0 START HORIZONTAL BLANK
9-bit Value = character clock value at which horizontal blanking begins. This register contains the least significant 8 bits of this value.

End Horizontal Blank Register (E_H_BLNK) (CR3)

Read/Write Address: 3?5H, Index 03H
Power-On Default: Undefined Paired

This register determines the pulse width of the $\overline{\text{BLANK}}$ signal and the display enable skew.

7	6	5	4	3	2	1	0
R	DSP-SKW 1	0	END HORIZONTAL BLANK				

Bits 4–0 END HORIZONTAL BLANK
7-bit Value = least significant 7 bits of the character clock counter value at which time horizontal blanking ends. To obtain this value, add the desired $\overline{\text{BLANK}}$ pulse width in character clocks to the Start Horizontal Blank value, which is also in character clocks. The 5 least significant bits of this sum are programmed into this field. The sixth bit is programmed into bit 7 of CR5. If the horizontal blank period is more than 64 character clocks, bit 3 of CR5D must be set to 1.

Bits 6–5 DSP-SKW - Display Skew
These two bits determine the amount of display enable skew. Display enable skew control provides sufficient time for the CRT Controller to access the display buffer to obtain a character and attribute code, access the character generator font, and then go through the Horizontal Pixel Panning register in the Attribute Controller. Each access requires the display enable signal to be skewed one character clock unit so the video output is synchronous with the HSYNC and VSYNC signals. The bit values and amount of skew are shown in the following table:
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 Reserved

Start Horizontal Sync Position Register (S_H_SY_P) (CR4)

Read/Write Address: 3?5H, Index 04H
Power-On Default: Undefined Paired

This register is used to adjust the screen center horizontally and to specify the character position at which HSYNC becomes active. Bit 8 of this value is bit 4 of CR5D.

7	6	5	4	3	2	1	0
START HORIZONTAL SYNC POSITION							

Bits 7–0 START HORIZONTAL SYNC POSITION.
9-bit Value = character clock counter value at which HSYNC becomes active. This register contains the least significant 8 bits of this value.

End Horizontal Sync Position Register (E_H_SY_P) (CR5)

Read/Write Address: 3?5H, Index 05H
Power-On Default: Undefined Paired

This register specifies when the HSYNC signal becomes inactive and the horizontal skew.

7	6	5	4	3	2	1	0
EHB b5	HOR-SKW 1	0	END HORIZONTAL SYNC POS				

Bits 4–0 END HORIZONTAL SYNC POS
6-bit Value = 6 least significant bits of the character clock counter value at which time HSYNC becomes inactive. To obtain this value, add the desired HSYNC pulse width in character clocks to the Start Horizontal Sync Position value, also in character clocks. The 5 least significant bits of this sum are programmed into this field. If the horizontal sync period is more than 32 character clocks, bit 5 of CR5D must be set to 1.

Bits 6–5 HOR-SKW - Horizontal Skew
These bits control the skew of the HSYNC signal. A binary 00 equals no HSYNC delay. For some modes, it is necessary to provide an HSYNC signal that takes up the entire blanking interval. Some internal timings are generated by the falling edge of the HSYNC signal. To guarantee the signals are latched properly, HSYNC is asserted before the end of the display enable signal, and then skewed several character clock times to provide the proper screen centering.
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 EHB b5
End Horizontal Blanking bit 5.

Vertical Total Register (V_TOTAL) (CR6)

Read/Write Address: 3?5H, Index 06H
Power-On Default: Undefined Paired

This register specifies the number of scan lines from one VSYNC active to the next VSYNC active. The scan line counter resets to 0 at this point. Bit 8 is bit 0 of CR7. Bit 9 is bit 5 of CR7. Bit 10 is bit 0 of CR5E.

7	6	5	4	3	2	1	0
VERTICAL TOTAL							

Bits 7–0 VERTICAL TOTAL
11-bit Value = (number of scan lines from VSYNC active to the next VSYNC active) - 2.
This register contains the least significant 8 bits of this value.

CRTC Overflow Register (OVFL_REG) (CR7)

Read/Write Address: 3?5H, Index 07H
Power-On Default: Undefined Paired except as noted

7	6	5	4	3	2	1	0
VRS 9	VDE 9	VT 9	LCM 8	SVB 8	VRS 8	VDE 8	VT 8

This register provides extension bits for fields in other registers.

Bit 0 Bit 8 of the Vertical Total register (CR6)

Bit 1 Bit 8 of the Vertical Display End register (CR12)

Bit 2 Bit 8 of the Vertical Retrace Start register (CR10)

Bit 3 Bit 8 of the Start Vertical Blank register (CR15)

Bit 4 Bit 8 of the Line Compare register (CR18) (not paired)

Bit 5 Bit 9 of the Vertical Total register (CR6)

Bit 6 Bit 9 of the Vertical Display End register (CR12)

Bit 7 Bit 9 of the Vertical Retrace Start register (CR10)

Preset Row Scan Register (P_R_SCAN) (CR8)

Read/Write Address: 3?5H, Index 08H
Power-On Default: Undefined

This register is used for the pixel scrolling and panning, and text formatting and vertical scrolling.

7	6	5	4	3	2	1	0
= 0	BYTE-PAN 1	0	PRE-SET ROW SCAN COUNT				

Bits 4–0 PRE-SET ROW SCAN COUNT
Value = starting row within a character cell for the first character row displayed after vertical retrace. This allows a partial character row to be displayed at the top of the display and is used for scrolling.

Bits 6–5 BYTE-PAN
Value = number of bytes to pan. The number of pixels to pan is specified in AR13.

Note: These bits are paired

Bit 7 Reserved = 0

Maximum Scan Line Register (MAX_S_LN) (CR9)

Read/Write Address: 3?5H, Index 09H
Power-On Default: Undefined

This register specifies the number of scan lines per character row and provides one scanning control bit and two overflow bits.

7	6	5	4	3	2	1	0
DBL SCN	LCM 9	SVB 9	MAX SCAN LINE				

Bits 4–0 MAX SCAN LINE
Value = (number of scan lines per character row) - 1

Bit 5 SVB 9
Bit 9 of the Start Vertical Blank Register (CR15)

Note: This bit is paired.

Bit 6 LCM 9
Bit 9 of the Line Compare Register (CR18)

Bit 7 DBL SCN
0 = Normal operation
1 = Enables double scanning operation. Each line is displayed twice by repeating the row scan counter and video memory address. Vertical parameters in the CRT controller are not affected.

Note: This bit is paired.

Cursor Start Scan Line Register (CSSL) (CRA)

Read/Write Address: 3?5H, Index 0AH
Power-On Default: Undefined

The cursor start register defines the row scan of a character line where the cursor begins.

7	6	5	4	3	2	1	0
= 0	= 0	CSR OFF	CSR CURSOR START SCAN LINE				

Bits 4–0 CSR CURSOR START SCAN LINE
Value = (starting cursor row within the character cell) - 1. When the cursor start register is programmed with a value greater than the cursor end register, no cursor is generated.

Bit 5 CSR OFF
0 = Turns on the text cursor
1 = Turns off the text cursor

Bits 7–6 Reserved = 0

Cursor End Scan Line Register (CESL) (CRB)

Read/Write Address: 3?5H, Index 0BH
Power-On Default: Undefined

This register defines the row scan of a character line where the cursor ends.

7	6	5	4	3	2	1	0
= 0	CSR-SKW 1	0	CURSOR END SCAN LINE				

Bits 4–0 CURSOR END SCAN LINE
Value = ending scan line number within the character cell for the text cursor. If the value of the cursor start scan line is greater than the value of cursor end line, then no cursor is generated.

Bits 6–5 CSR-SKW - Cursor Skew
These bits control the delay skew of the cursor signal. Cursor skew delays the text cursor by the selected number of clocks. For example, a skew of 1 moves the cursor right one character position on the screen.
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 Reserved = 0

Start Address High Register (STA(H)) (CRC)

Read/Write Address: 3?5H, Index 0CH
Power-On Default: Undefined Paired

15	14	13	12	11	10	9	8
DISPLAY START ADDRESS (HIGH)							

20-bit Value = the first address after a vertical retrace at which the display on the screen begins on each screen refresh. These along with bits 3-0 of CR69 are the high order start address bits.

Start Address Low Register (STA(L)) (CRD)

Read/Write Address: 3?5H, Index 0DH
Power-On Default: Undefined Paired

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS (LOW)							

Start address (low) contains the 8 low order bits of the address.

Cursor Location Address High Register (CLA(H)) (CRE)

Read/Write Address: 3?5H, Index 0EH
Power-On Default: Undefined

15	14	13	12	11	10	9	8
CURSOR LOCATION ADDRESS (HIGH)							

20-bit Value = the cursor location address of the video memory where the text cursor is active. This register along with bits 2-0 of CR69 are the high order bits of the address.

Cursor Location Address Low Register (CLA(L)) (CRF)

Read/Write Address: 3?5H, Index 0FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
CURSOR LOCATION ADDRESS (LOW)							

Cursor location address (low) contains the 8 low order bits of the address.

Vertical Retrace Start Register (VRS) (CR10)

Read/Write Address: 3?5H, Index 10H
Power-On Default: Undefined Paired

7	6	5	4	3	2	1	0
VERTICAL RETRACE START							

Bits 7–0 VERTICAL RETRACE START.
11-bit Value = scan line counter value at which VSYNC becomes active. These are the low-order 8 bits. Bit 8 is bit 2 of CR7. Bit 9 is bit 7 of CR7. Bit 10 is bit 4 of CR5E.

Vertical Retrace End Register (VRE) (CR11)

Read/Write Address: 3?5H, Index 11H
Power-On Default: 0xH

This register controls the vertical interrupt and CR0-7

7	6	5	4	3	2	1	0
LOCK R0-7	REF 3/5	DIS VINT	CLR VINT	VERTICAL RETRACE END			

Bits 3–0 VERTICAL RETRACE END
Value = least significant 4 bits of the scan line counter value at which VSYNC goes inactive. To obtain this value, add the desired VSYNC pulse width in scan line units to the CR10 value, also in scan line units. The 4 least significant bits of this sum are programmed into this field. This allows a maximum VSYNC pulse width of 15 scan line units.

Note: These bits are paired

Bit 4 $\overline{\text{CLR}}$ VINT - Clear Vertical Retrace Interrupt
0 = Vertical retrace interrupt cleared
1 = The flip-flop is able to catch the next interrupt request

At the end of active vertical display time, a flip-flop is set for a vertical interrupt. The output of this flip-flop goes to the system interrupt controller. The CPU has to reset this flip-flop by writing a logical 0 to this bit while in the interrupt process, then set the bit to 1 to allow the flip-flop to catch the next interrupt request. Do not change the other bits in this register. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on.

Bit 5 DIS VINT - Disable Vertical Interrupt
0 = Vertical retrace interrupt enabled if CR32_4 = 1
1 = Vertical interrupt disabled. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on

Bit 6 REF $\overline{3}$/5 - Refresh Cycle Select
0 = Three DRAM refresh cycles generated per horizontal line
1 = Five DRAM refresh cycles generated per horizontal line. Selecting five refresh cycles allows use of the VGA chip with slow sweep rate displays (15.75 KHz). This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on. This setting can be overridden via bits 1-0 of CR3A

Bit 7 LOCK R0-7 - Lock Writes to CRT Controller Registers
0 = Writing to all CRT Controller registers enabled
1 = Writing to all bits of the CRT Controller registers CR0–CR7 except bit 4 of CR7 (LCM8) disabled. This bit is set to 1 by the BIOS during a mode set, a reset or power-on

Note: This bit is paired.

Vertical Display End Register (VDE) (CR12)

Read/Write Address: 3?5H, Index 12H
Power-On Default: Undefined

The vertical display enable end register defines 8 bits of the 10-bit address of the scan line where the display on the screen ends. Bit 8 and Bit 9 are bits 1 and 6 of CR7. Bit 10 is bit 1 of CR5E. This register is locked/unlocked via CR35_7.

7	6	5	4	3	2	1	0
VERTICAL DISPLAY END							

Bit 7–0 VERTICAL DISPLAY END
11-bit Value = (number of scan lines of active display) - 1. This register contains the least significant 8 bits of this value.

Offset Register (SCREEN-OFFSET) (CR13)

Read/Write Address: 3?5H, Index 13H
Power-On Default: Undefined Paired

This register specifies the logical line width of the screen and is sometimes called the screen pitch. The starting memory address for the next display row is larger than the current row by two, four or eight times this amount. Bits 5-4 of CR51 are extension bits 9-8 of this register.

7	6	5	4	3	2	1	0
LOGICAL SCREEN WIDTH							

Bits 7–0 LOGICAL SCREEN WIDTH
10-bit Value = quantity that is multiplied by 2 (word mode), 4 (doubleword mode) or 8 (quadword mode) to specify the difference between the starting byte addresses of two consecutive scan lines. This register contains the least significant 8 bits of this value. The addressing mode is specified by bit 6 of CR14 and bit 3 of CR17. Setting bit 3 of CR31 to 1 forces doubleword mode.

Underline Location Register (ULL) (CR14)

Read/Write Address: 3?5H, Index 14H
Power-On Default: Undefined

This register specifies the horizontal row scan position of underline and display buffer addressing modes.

7	6	5	4	3	2	1	0
= 0	DBWD MODE	CNT BY4	UNDER LINE LOCATION				

Bits 4–0 UNDER LINE LOCATION
5-bit Value = (scan line count of a character row on which an underline occurs) -1

Bit 5 CNT BY4 - Select Count by 4 Mode
0 = The memory address counter depends on bit 3 of CR17 (count by 2)
1 = The memory address counter is incremented every four character clocks

The CNT BY4 bit is used when double word addresses are used.

Bit 6 DBLWD MODE - Select Doubleword Mode
0 = The memory addresses are byte or word addresses
1 = The memory addresses are doubleword addresses

Bit 7 Reserved = 0

Start Vertical Blank Register (SVB) (CR15)

Read/Write Address: 3?5H, Index 15H
Power-On Default: Undefined Paired

This register specifies the scan line at which the vertical blanking period begins. Bit 8 is bit 3 of CR7. Bit 9 is bit 5 of CR9. Bit 10 is bit 2 of CR5E.

7	6	5	4	3	2	1	0
START VERTICAL BLANK							

Bits 7–0 START VERTICAL BLANK.
11-bit value = (scan line count at which $\overline{\text{BLANK}}$ becomes active) - 1. This register contains the least significant 8 bits of this value.

End Vertical Blank Register (EVB) (CR16)

Read/Write Address: 3?5H, Index 16H
Power-On Default: Undefined Paired

This register specifies the scan line count value when the vertical blank period ends.

7	6	5	4	3	2	1	0
END VERTICAL BLANK							

Bits 7–0 END VERTICAL BLANK
Value = least significant 8 bits of the scan line counter value at which vertical blanking ends. To obtain this value, add the desired width of the vertical blanking pulse in scan lines to the value in the Start Vertical Blank register, also in scan lines. The 8 least significant bits of this sum are programmed into this field. This allows a maximum vertical blanking pulse of 255 scan line units.

For TV modes, the value programmed in CR6 (the 8 LSBs of the vertical total) should also be programmed in this register.

CRTC Mode Control Register (CRT_MD) (CR17)

Read/Write Address: 3?5H, Index 17H
Power-On Default: 00H

This register is a multifunction control register, with each bit defining a different specification.

7	6	5	4	3	2	1	0
RST	BYTE MODE	ADW 16K	= 0	WRD MODE	VT X2	4BK HGC	2BK CGA

Bit 0 $\overline{2BK}$ CGA - Select Bank 2 Mode for CGA Emulation
0 = Row scan counter bit 0 is substituted for memory address bit 13 during active display time
1 = Memory address bit 13 appears on the memory address output bit 13 signal of the CRT controller

This bit allows memory mapping compatibility with the IBM CGA graphics mode.

Bit 1 $\overline{4BK}$ HGC - Select Bank 4 Mode for HGA Emulation
0 = Row scan counter bit 1 is substituted for memory address bit 14 during active display time
1 = Memory address bit 14 appears on the memory address output bit 14 signal of the CRT controller

The combination of this bit and bit 0 of this register allows compatibility with Hercules HGC graphics memory mapping.

Bit 2 VT X2 - Select Vertical Total Double Mode
0 = Horizontal retrace clock selected
1 = Horizontal retrace clock divided by two selected

This bit selects horizontal retrace clock or horizontal retrace clock divided by two as the clock that controls the vertical timing counter. If the vertical retrace counter is clocked with the horizontal retrace clock divided by 2, then the vertical resolution is double.

Note: This bit is paired.

Bit 3 CNT BY2 - Select Word Mode
0 = Memory address counter is clocked with the character clock input, and byte mode addressing for the video memory is selected
1 = Memory address counter is clocked by the character clock input divided by 2, and word mode addressing for the video memory is selected

Bit 4 Reserved = 0

Bit 5 $\overline{\text{ADW}}$ 16K - Address Wrap
0 = When word mode is selected by bit 6 of this register, memory address counter bit 13 appears on the memory address output bit 0 signal of the CRT controller and the video memory address wraps around at 16 KBytes
1 = When word mode is selected by bit 6 of this register, memory address counter bit 15 appears on the memory address output bit 0 signal of the CRT controller

This bit is useful in implementing IBM CGA mode.

Bit 6 BYTE MODE - Select Byte Addressing Mode
0 = Word mode shifts all memory address counter bits down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output
1 = Byte address mode

Bit 7 $\overline{\text{RST}}$ - Hardware Reset
0 = Vertical and horizontal retrace pulses always inactive
1 = Vertical and horizontal retrace pulses enabled

This bit does not reset any other registers or outputs.

Note: This bit is paired.

Line Compare Register (LCM) (CR18)

Read/Write Address: 3?5H, Index 18H
Power-On Default: Undefined

This register is used to implement a split screen function. When the scan line counter value is equal to the content of this register, the memory address counter is cleared to 0. The linear address counter then sequentially addresses the display buffer starting at address 0. Each subsequent row address is determined by the addition of the Offset (CR13) register content. Bit 8 is bit 4 of CR7. Bit 9 is bit 6 of CR9. Bit 10 is bit 6 of CR5E.

7	6	5	4	3	2	1	0
LINE COMPARE POSITION							

Bit 7–0 LINE COMPARE POSITION
11-bit Value = number of scan lines at which the screen is split into screen A and screen B. This register contains the least significant 8 bits of this value.

CPU Latch Data Register (GCCL) (CR22)

Read Only Address: 3?5H, Index 22H
Power-On Default: Undefined

This register is used to read the CPU latch in the Graphics Controller. CR39 must be programmed to A0H in order for this register to be read.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER CPU LATCH - N							

Bits 7–0 GRAPHICS CONTROLLER CPU LATCH - N
Bits 1-0 of GR4 select the latch number N (3-0) of the CPU Latch.

Attribute Index Register (ATC_F/I) (CR24)

Read Only Address: 3?5H, Index 24H, 26H
Power-On Default: Undefined

This register is used to read the value of the Attribute Controller Index register and its associated internal address flip-flop (AFF). It can be read at either index 24H or 26H. CR39 must be programmed to A0H in order for this register to be read.

7	6	5	4	3	2	1	0
AFF	= 0	ENV	ATTRIBUTE CONTROLLER INDEX				

Bits 4–0 ATTRIBUTE CONTROLLER INDEX
This value is the Attribute Controller Index Data at I/O port 3C0H.

Bit 5 ENV- Enable Video Display
This is the setting of bit 5 of 3C0H, indicating video display enabled status (1 = enabled).

Bit 6 Reserved = 0

Bit 7 $\overline{\text{AFF}}$
Inverted Internal Address flip-flop

16.4 GRAPHICS CONTROLLER REGISTERS

The graphics controller registers are located at a two byte I/O address space. These registers are accessed by first writing an index to the Graphics Address register (at 3CEH) and then accessing the Data register (at 3CFH).

Graphics Controller Index Register (GRC_ADR)

Read/Write Address: 3CEH
Power-On Default: Undefined

This register is loaded with a binary index value that determines which graphics controller register will be accessed. This value is referred to as the "Index Number" of the GR register (GR0–6).

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	GR CONT ADDRESS			

Bits 3–0 GR CONT ADDRESS - Graphics Controller Register Index
A binary value indexing the register where data is to be accessed.

Bits 7–4 Reserved = 0

Graphics Controller Data Register (GRC_DATA)

Read/Write Address: 3CFH
Power-On Default: Undefined

This register is the data port for the graphics controller register indexed by the Graphics Controller Index register.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER DATA							

Bit 7–0 GRAPHICS CONTROLLER DATA
Data to the Graphics Controller register indexed by the graphics controller address.

Set/Reset Data Register (SET/RST_DT) (GR0)

Read/Write Address: 3CFH, Index 00H
Power-On Default: Undefined

This register represents the value written to all 8 bits of the respective memory plane when the CPU executes a memory write in write modes 0 and 3.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	SET/RESET DATA			

Bits 3–0 SET/RESET DATA
These bits become the color value for CPU memory write operations. In write mode 0, the set/reset data can be enabled on the corresponding bit of the Enable Set/Reset Data register. In write mode 3, there is no effect on the Enable Set/Reset Data register.

Bits 7–4 Reserved = 0

Enable Set/Reset Data Register (EN_S/R_DT) (GR1)

Read/Write Address: 3CFH, Index 01H
Power-On Default: Undefined

These bits enable the set/reset data, and affect write mode 0.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	ENB SET/RST DATA			

Bits 3–0 ENB SET/RST DATA
When each bit is a logical 1, the respective memory plane is written with the value of the Set/Reset Data register. A logical 0 disables the set/reset data in a plane, and that plane is written with the value of CPU write data.

Bits 7–4 Reserved = 0

Color Compare Register (COLOR-CMP) (GR2)

Read/Write Address: 3CFH, Index 02H
Power-On Default: Undefined

These bits represent a 4-bit color value to be compared. In read mode 1, the CPU executes a memory read, the read data is compared with this value and returns the results. This register works in conjunction with the Color Don't Care register.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	COLOR COMPARE DATA			

Bits 3–0 COLOR COMPARE DATA
This value becomes the reference color used to compare each pixel. Each of the 8-bit positions of the read data are compared across four planes and a logical 1 is returned in each bit position for which the colors match.

Bits 7–4 Reserved = 0

Raster Operation/Rotate Count Register (WT_ROP/RTC) (GR3)

Read/Write Address: 3CFH, Index 03H
Power-On Default: Undefined

This register selects a raster operation function and indicates the number of bits the CPU data will be rotated (right) on the video memory write operation.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	RST-OP 1	0	ROTATE-COUNT		

Bits 2–0 ROTATE-COUNT
These bits define a binary encoded value of the number of positions to right-rotate data during a CPU memory write. To write non-rotated data, the CPU must preset a count of 0.

Bits 4–3 RST-OP - Select Raster Operation
The data written to memory can operate logically with the data already in the processor latches. This function is not available in write mode 1. The logical functions are defined as follows:
00 = No operation
01 = Logical AND with latched data
10 = Logical OR with latched data
11 = Logical XOR with latched data

The logical function specified by this register is applied to data being written to memory while in modes 0, 2 and 3.

Bits 7–5 Reserved = 0

Read Plane Select Register (RD_PL_SL) (GR4)

Read/Write Address: 3CFH, Index 04H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
						RD-PL-SL	
= 0	= 0	= 0	= 0	= 0	= 0	1	0

The contents of this register represent the memory plane from which the CPU reads data in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored. Four memory planes are selected as follows:

Bits 1–0 RD-PL-SL - Read Plane Select
The memory plane is selected as follows:
00 = Plane 0
01 = Plane 1
10 = Plane 2
11 = Plane 3

Bits 7–2 Reserved = 0

Graphics Controller Mode Register (GRP_MODE) (GR5)

Read/Write Address: 3CFH, Index 05H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
	SHF-MODE		O/E	RD		WRT-MD	
= 0	256	O/E	MAP	CMP	= 0	1	0

This register controls the mode of the Graphics Controller as follows:

Bit 1–0 WRT-MD - Select Write Mode
These bits select the CPU write mode into video memory. The function of each mode is defined as follows:
00 = Write Mode 0. Each of four video memory planes is written with the CPU data rotated by the number of counts in the rotate register. If the Set/Reset register is enabled for any of four planes, the corresponding plane is written with the data stored in the set/reset register. Raster operations and bit mask registers are effective
01 = Write Mode 1. Each of four video memory planes is written with the data in the processor latches. These latches are loaded during previous CPU read operations. Raster operation, rotate count, set/reset data, enable set/reset data and bit mask registers are not effective
10 = Write Mode 2. Memory planes 0-3 are filled with 8 bits of the value of CPU write data bits 0-3, respectively. For example, if write data bit 0 is a 1, eight 1's are written to memory plane 0. The data on the CPU data bus is treated as the color value. The Bit Mask register is effective as the Mask register. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A logical 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset, Enable Set/Reset and Rotate Count registers are ignored
11 = Write Mode 3. Each of four video memory planes is written with 8 bits of the color value contained in the set/reset register for that plane. The Enable Set/Reset register is not effective. Rotated CPU write data is ANDed with the bit mask register to form an 8-bit value that performs the same function as the Bit Mask register in write modes 0 and 2. This write mode can be used to fill an area with a single color and pattern

Bit 2 Reserved = 0

Bit 3 RD CMP - Enable Read Compare
0 = The CPU reads data from the video memory planes. The plane is selected by the Read Plane Select register. This is called read mode 0
1 = The CPU reads the results of the logical comparison between the data in four video memory planes selected by the contents of the Color Don't Care register and the contents of the Color Compare register. The result is a 1 for a match and 0 for a mismatch on each pixel. This is called read mode 1

Bit 4 O/E MAP - Select Odd/Even Addressing
0 = Standard addressing.
1 = Odd/even addressing mode selected. Even CPU addresses access plane 0 and 2, while odd CPU addresses access plane 1 and 3. This option is useful for emulating the CGA compatible mode. The value of this bit should be the inverted value programmed in bit 2 of the Sequencer Memory Mode register (SR4). This bit affects reading of display memory by the CPU

Bit 5 SHF-MODE - Select Odd/Even Shift Mode
0 = Normal shift mode
1 = The video shift registers in the graphics section are directed to format the serial data stream with even-numbered bits from both planes on the even-numbered planes and odd-numbered bits from both planes on the odd planes

Bit 6 SHF-MODE - Select 256 Color Shift Mode
0 = Bit 5 in this register controls operation of the video shift registers
1 = The shift registers are loaded in a manner that supports the 256 color mode

Bit 7 Reserved = 0

Memory Map Mode Control Register (MISC_GM) (GR6)

Read/Write Address: 3CFH, Index 06H
Power-On Default: Undefined

This register controls the video memory addressing.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	MEM-MAP 1	MEM-MAP 0	CHN O/E	TXT /GR

Bit 0 $\overline{\text{TXT}}$/GR - Select Text/Graphics Mode
0 = Text mode display addressing selected
1 = Graphics mode display addressing selected. When set to graphics mode, the character generator address latches are disabled

Bit 1 CHN O/E - Chain Odd/Even Planes
0 = A0 address bit unchanged
1 = CPU address bit A0 is replaced by a higher order address bit. The content of A0 determines which memory plane is to be addressed. A0 = 0 selects planes 0 and 2, and A0 = 1 selects planes 1 and 3. This mode can be used to double the address space into video memory

Bits 3–2 MEM-MAP - Memory Map Mode
These bits control the address mapping of video memory into the CPU address space. The bit functions are defined below.
00 = A0000H to BFFFFH (128 KBytes)
01 = A0000H to AFFFFH (64 KBytes)
10 = B0000H to B7FFFH (32 KBytes)
11 = B8000H to BFFFFH (32 KBytes)

Bits 7–4 Reserved = 0

Color Don't Care Register (CMP_DNTC) (GR7)

Read/Write Address: 3CFH, Index 07H
Power-On Default: Undefined

This register is effective in read mode 1, and controls whether the corresponding bit of the Color Compare Register is to be ignored or used for color comparison.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	COMPARE PLANE SEL			

Bits 3–0 COMPARE PLANE SEL - Compare Plane Select
0 = The corresponding color plane becomes a don't care plane when the CPU read from the video memory is performed in read mode 1
1 = The corresponding color plane is used for color comparison with the data in the Color Compare register

Bits 7–4 Reserved = 0

Bit Mask Register (BIT_MASK) (GR8)

Read/Write Address: 3CFH, Index 08H
Power-On Default: Undefined

Any bit programmed to 0 in this register will cause the corresponding bit in each of four memory planes to be immune to change. The data written into memory in this case is the data which was read in the previous cycle, and was stored in the processor latches. Any bit programmed to 1 allows unimpeded writes to the corresponding bits in the plane.

7	6	5	4	3	2	1	0
BIT MASK							

Bits 7–0 BIT MASK
A logical 0 means the corresponding bit of each plane in memory is set to the corresponding bit in the processor latches. A logical 1 means the corresponding bit of each plane in memory is set as specified by other conditions.

16.5 ATTRIBUTE CONTROLLER REGISTERS

The attribute controller registers are located at the same byte I/O address for writing address and data. An internal address flip-flop (AFF) controls the selection of either the attribute index or data registers. To initialize the address flip-flop (AFF), an I/O read is issued at address 3BAH or 3DAH. This presets the address flip-flop to select the index register. After the index register has been loaded by an I/O write to address 3C0H, AFF toggles and the next I/O write loads the data register. Every I/O write to address 3C0H toggles this address flip-flop. However, it does not toggle for I/O reads at address 3C0H or 3C1H. The Attribute Controller Index register is read at 3C0H, and the Attribute Controller Data register is read at address 3C1H.

Attribute Controller Index Register (ATR_AD)

Read/Write Address: 3C0H
Power-On Default: Undefined

This register is loaded with a binary index value that determines which attribute controller register will be accessed. This value is referred to as the "Index Number" of the AR register (AR0–14).

7	6	5	4	3	2	1	0
R	R	ENB PLT	ATTRIBUTE ADDRESS				

Bits 4–0 ATTRIBUTE ADDRESS
A binary value that points to the attribute controller register where data is to be written.

Bit 5 ENB PLT - Enable Video Display
0 = Video display access to the palette registers disabled. The Attribute Controller register can be accessed by the CPU
1 = Display video using the palette registers enabled (normal display operation). The palette registers (AR0–ARF) cannot be accessed by the CPU

This bit is effective only in 8-bit PA mode (CR67_4 = 0).

Bits 7–6 Reserved

Attribute Controller Data Register (ATR_DATA)

Read/Write Address: R: 3C1H/W: 3COH
Power-On Default: Undefined

This register is the data port for the attribute controller register indexed by the Attribute Controller Index register.

7	6	5	4	3	2	1	0
ATTRIBUTE DATA							

Bits 7–0 ATTRIBUTE DATA
Data to the attribute controller register indexed by the attribute controller address.

Palette Registers (PLT_REG) (AR00-0F)

Read/Write Address: 3C1H/3C0H, Index 00H-0FH
Power-On Default: Undefined

These are 16, 6-bit registers pointed to by the index and color code. They allow a dynamic mapping between the text attribute or graphics color input and the display color on the CRT screen.

7	6	5	4	3	2	1	0
		SECONDARY			PRIMARY		
= 0	= 0	SR	SG	SB	R	G	B

Bits 5–0 PALETTE COLOR
The six bit display color, bits 5-0 are output as SR, SG/I, SB/V, R, G and B, respectively.

Bits 7–6 Reserved = 0

Attribute Mode Control Register (ATR_MODE) (AR10)

Read/Write Address: 3C1H/3C0H, Index 10H
Power-On Default: 00H

The contents of this register controls the attribute mode of the display function.

7	6	5	4	3	2	1	0
SEL V54	256 CLR	TOP PAN	= 0	ENB BLNK	ENB LGC	MONO ATRB	TX /GR

Bit 0 $\overline{TX}$/GR - Select Graphics Mode
0 = Selects text attribute control mode
1 = Selects graphics control mode

Bit 1 MONO ATRB - Select Monochrome Attributes
0 = Selects color display text attributes
1 = Selects monochrome display text attributes

Bit 2 ENB LGC - Enable Line Graphics
0 = The ninth dot of a text character (bit 0 of SR1 = 0) is the same as the background
1 = Special line graphics character codes enabled

When this bit is set to 1, it forces the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes are C0H through DFH. For other characters, the ninth dot is the same as the background.

Bit 3 ENB BLNK - Enable Blinking
0 = Selects the background intensity for the text attribute input
1 = Selects blink attribute in text modes

This bit must also be set to 1 for blinking graphics modes. The blinking counter is operated by the vertical retrace counter (VRTC) input. It divides the VRTC input by 32. The blinking rates are ON for 16 VRTC clocks and OFF for 16 VRTC clocks. In the graphics mode, when blink is activated, the most significant color bit (bit 3) for each dot is inverted alternately, thus allowing two different colors to be displayed for 16 VRTC clocks each.

When the cursor is displayed in the text mode, it is blinked at a rate of ON for 8 VRTC clocks and OFF for 8 VRTC clocks (period by 16 frames). The displayed characters are independently blinked at the rate of 32 frames as above.

Bit 4 Reserved = 0

Bit 5 TOP PAN - Top Panning Enable
0 = Line compare has no effect on the output of the pixel panning register
1 = Forces the output of the pixel panning register to 0 after matching line compare until VSYNC occurs in the CRT controller. At the top of screen the output of the Pixel Panning register returns to its programmed value. This bit allows a top portion of a split screen to be panned.

Bit 6 256 CLR - Select 256 Color Mode
0 = 4 bits of video (translated to 6 bits by the palette) are output every internal dot-clock cycle
1 = Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot-clock

Bit 7 SEL V54 - Select V[5:4]
0 = In VGA, mode, bits 5-4 of video output are generated by the attribute palette registers. Bits 7-6 of video output are always generated by bits 3-2 of AR14
1 = Bits 5-4 of video output are generated by bits 1-0 of AR14

Border Color Register (BDR_CLR) (AR11)

Read/Write Address: 3C1H/3C0H, Index 11H
Power-On Default: 00H

7	6	5	4	3	2	1	0
BORDER COLOR							

Bits 7–0 Border Color. This 8-bit register determines the border color displayed on the CRT screen. The border is an area around the screen display area.

This register is only effective in 8-bit PA modes (CR67_4 = 0). See also CR33_5.

Color Plane Enable Register (DISP_PLN) (AR12)

Read/Write Address: 3C1H/3C0H, Index 12H
Power-On Default: 00H

This register enables the respective video memory color plane 3–0 and selects video color outputs to be read back in the display status.

7	6	5	4	3	2	1	0
= 0	= 0	VDT-SEL 1	0	DISPLAY PLANE ENBL			

Bits 3–0 DISPLAY PLANE ENBL
A 0 in any of these bits forces the corresponding color plane bit to 0 before accessing the internal palette. A 1 in any of these bits enables the data on the corresponding color plane.

Bits 5–4 VDT-SEL - Video Test Select
These bits select two of the eight bit color outputs to be available in the Input Status 1 register. The output color combinations available on the status bits are as follows:

D STS MUX		STS 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	Video 2	Video 0
0	1	Video 5	Video 4
1	0	Video 3	Video 1
1	1	Video 7	Video 6

Bits 7–6 Reserved = 0

Horizontal Pixel Panning Register (H_PX_PAN) (AR13)

Read/Write Address: 3C1H/3C0H, Index 13H
Power-On Default: 00H

This register specifies the number of pixels to shift the display data horizontally to the left. Pixel panning is available in both text and graphics modes. It is not available with Enhanced mode memory mappings (CR31_3 = 1).

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	NUMBER OF PAN SHIFT			

Bits 3–0 NUMBER OF PAN SHIFT
This register selects the number of pixels to shift the display data horizontally to the left. In the 9 pixels/character text mode, the output can be shifted a maximum shift of 8 pixels. In the 8 pixels/character text mode and all graphics modes, except 256 color mode, a maximum shift of 7 pixels is possible. In the 256 color mode, bit 0 of this register must be 0 resulting in only 4 panning positions per display byte. The panning is controlled as follows:

	Number of pixels shifted in		
Bits 3–0	**9 pixel/char.**	**8 pixel/char.**	**256 color mode**
0000	1	0	0
0001	2	1	–
0010	3	2	1
0011	4	3	–
0100	5	4	2
0101	6	5	–
0110	7	6	3
0111	8	7	–
1000	0	–	–

Bits 7–4 Reserved = 0

Pixel Padding Register (PX_PADD) (AR14)

Read/Write Address: 3C1H/3C0H, Index 14H
Power-On Default: 00H

This register specifies the high-order bits of video output when pixel padding is enabled and disabled in the 256 color mode.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	PIXEL PADDING V7	V6	V5	V4

Bits 1–0 PIXEL PADDING V5, V4
These bits are enabled with a logical 1 of bit 7 of AR10, and can be used in place of the V5 and V4 bits from the Palette registers to form the 8-bit digital color value output.

Bits 3–2 PIXEL PADDING V7, V6
In all modes except 256 color mode, these bits are the two high-order bits of the 8-bit digital color value output.

Bits 7–4 Reserved = 0

16.6 DAC REGISTERS

DAC Mask Register (DAC_AD_MK)

Read/Write Address: 3C6H
Power-On Default: Undefined

The CPU can access this register at any time.

7	6	5	4	3	2	1	0
DAC ADDRESS MASK							

Bits 7–0 DAC ADDRESS MASK
The contents of this register are bit-wise logically ANDed with the CLUT address. This register is initialized to FFH by the BIOS during a video mode set.

DAC Read Index Register (DAC_RD_AD)

Write Only Address: 3C7H
Power-On Default: Undefined

This register contains the pointer to one of 256 palette data registers and is used when reading the color palette.

7	6	5	4	3	2	1	0
DAC READ ADDRESS							

Bits 7–0 DAC READ ADDRESS
Each time the color code is written to this register, it identifies that a read sequence will occur. A read sequence consists of three successive byte reads from the DAC data register at I/O address 3C9H. The least significant 6 bits of each byte taken from the DAC data register contain the corresponding color value, and the most significant 2 bits contain zeros. The order is red byte first, then green, and finally blue. The sequence of events for a read cycle is:

1. Write the color code to this register (DAC Read Index) at address 3C7H.
2. The contents of the location in the color look-up table pointed to by the color code are transferred to the DAC data register at address 3C9H.
3. Three bytes are read back from the DAC data register.
4. The contents of this register auto-increment by one.
5. Go to step 2.

The effects of writing to the DAC data register during a three-byte read cycle or reading from the DAC data register during a 3-byte write cycle (i.e., interrupting the sequence) are undefined and may change the look-up table contents.

DAC Status Register (DAC_STS)

Read Only Address: 3C7H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	DAC-STS	

Bits 1–0 DAC-STS - DAC Cycle Status
The last executing cycle was:
00 = Write Palette cycle
11 = Read Palette cycle

Reads from the DAC Write Index at address 3C8H or the DAC status register at address 3C7H do not interfere with read or write cycles and may take place at any time.

Bits 7–2 Reserved = 0

DAC Write Index Register (DAC_WR_AD)

Read/Write Address: 3C8H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
DAC WRITE ADDRESS							

Bits 7–0 DAC WRITE ADDRESS
This register contains the pointer to one of 256 palette data registers and is used during a palette load. Each time the color code is written to this register, it identifies that a write sequence will occur. A write sequence consists of three successive byte writes to the DAC data register at I/O address 3C9H. The least significant 6 bits of each byte are concatenated to form the value placed in the 18-bit data register. The order is red byte first, then green, and finally blue. Once the third byte has been written, the value in the data register is written to the location pointed to by the color code. The sequence of events for a write cycle is:

1. Write the color code to this register (DAC Write Index) at address 3C8H.
2. Three bytes are written to the DAC Data register at address 3C9H.
3. The contents of the DAC data register are transferred to the location in the color look-up table pointed to by the color code.
4. The DAC Write Index register auto-increments by 1.
5. Go to step 2.

DAC Data Register (DAC_DATA)

Read/Write Address: 3C9H
Power-On Default: Undefined

This register is a data port to read or write the contents of the location in the color look-up table pointed to by the DAC Read Index or the DAC Write Index registers.

7	6	5	4	3	2	1	0
DAC READ/WRITE DATA							

Bits 7–0 DAC READ/WRITE DATA
To prevent "snow flicker" on the screen, an application reading data from or writing data to the DAC Data register should ensure that the $\overline{\text{BLANK}}$ input to the DAC is asserted. This can be accomplished either by restricting data transfers to retrace intervals, checking bit 3 of the Input Status 1 register (3?AH) to determine when retrace is occurring, or by using the screen-off bit in the Clocking Mode register of the sequencer (bit 5 of SR1).

Section 17: Extended Sequencer Register Descriptions

The following registers are located in Sequencer Register address space not used by standard VGA. An appropriate value must be programmed in SR8 to unlock access to these registers.

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). See Appendix A for a table listing each register in this section and its page number.

Unlock Extended Sequencer Register (SR8)

Read/Write Address: 3C5H, Index 08H
Power-On Default: 00H

Loading xxxx0110b (e.g., 06H) unlocks accessing of all the S3 extensions (SR9 and above) to the standard VGA Sequencer register set. (x = don't care).

7	6	5	4	3	2	1	0
R	R	R	R	=0	=1	=1	=0

Extended Sequencer 9 Register (SR9)

Read/Write Address: 3C5H, Index 09H
Power-On Default: 00H

This register controls the powerdown for the Controller 1 dot clock (DCLK). There are two types of DCLK used in Controller 1: the virtual DCLK is used on logic which is affected by flat panel horizontal expansion while the true DCLK is used on logic which is not affected by flat panel horizontal expansion.

7	6	5	4	3	2	1	0
MMIO	C1SU2	C1SB2	C1SU1	C1SB1	C1P1	EPD	R

Bit 0 Reserved

Bit 1 EPD - Engine Power Down Control
0 = S3d engine clock is enabled at all times
1 = S3d engine clock is powered down when the engine is not busy

Bit 2 C1P1 - Controller 1 Powerdown Enable 1
0 = Controller 1 virtual DCLK is not turned off when CR67_2=1
1 = Controller 1 virtual DCLK is turned off when CR67_2=1

This bit should be programmed to 1 by the BIOS during reset.

Bit 3 C1SB1 - Controller 1 Standby Enable 1
0= Controller 1 virtual DCLK is not turned off in Standby mode
1= Controller 1 virtual DCLK is turned off in Standby mode

This bit should be programmed to 1 by the BIOS during reset.

Bit 4 C1SU1 - Controller 1 Suspend Enable 1
0 = Controller 1 virtual DCLK is not turned off in Suspend mode
1 = Controller 1 virtual DCLK is turned off in Suspend mode

This bit should be programmed to 1 by the BIOS during reset.

Bit 5 Controller 1 Standby Enable 2
0 = Controller 1 true DCLK is not turned off in Standby mode
1 = Controller 1 true DCLK is turned off in Standby mode

This bit should be programmed to 1 by the BIOS during reset.

Bit 6 Controller 1 Suspend Enable 2
0 = Controller 1 true DCLK is not turned off in Suspend mode
1 = Controller 1 true DCLK is turned off in Suspend mode

This bit should be programmed to 1 by the BIOS during reset.

Bit 7 MMIO-ONLY - Memory-mapped I/O register access only
0 = When MMIO is enabled, both programmed I/O and memory-mapped I/O register accesses are allowed
1 = When MMIO is enabled, only memory-mapped I/O register accesses are allowed to extended (non-standard VGA) registers. Both I/O and MMIO accesses can be made to standard VGA registers.

Extended Sequencer A Register (SRA)

Read/Write Address: 3C5H, Index 0AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	ES3d	DRF	D2D	24B	16B	R	ADO

Bit 0 ADO - AD[31:0] Output Strength
0 = 8 mA
1 = 16 mA

Bit 1 Reserved

Bit 2 16B - Enable 16 BPP Fix
0 = 16 BPP fix disabled
1 = 16 BPP fix enabled

Bit 3 24B - Enable 24 BPP Alpha Blending Fix
0 = 24 BPP fix disabled
1 = 24 BPP fix enabled

Bit 4 D2D - Delay 2D/3D Command
0 = No delay
1 = Delay 2D command when is it is following a 3D command or delay 3D command when it is following a 2D command

Bit 5 DRF - Delay Rectangle Fill or Line Draw
0 = No delay
1 = Delay rectangle fill or line draw command when it is following a 3D command

Bits 6 ES3d - Extend S3d Engine Busy
0 = Extend S3d engine busy signal is not extended
1 = Extend S3d engine busy signal by at least one 32 kHz clock

This may be used to ensure that the engine clock is not shut off while data is still in the engine pipeline when SR9_1 = 1.

Bit 7 Reserved

DCLK2 Control Register (SRB)

Read/Write Address: 3C5H, Index 0BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
ED2S	IC2D	D2RC	D2B2	TB1	DOS	D2L	PD2

Bit 0 PD2 - Power Down DCLK2 PLL
0 = DCLK2 PLL is not powered down
1 = DCLK2 PLL is powered down

Bit 1 D2L - Enable New DCLK2 Frequency Load
0 = Register bit clear
1 = Load new DCLK2 frequency.

When new DCLK2 PLL values are programmed, this bit is set to 1 to load these values in the PLL. When DCLK2 is selected to clock controller 1, 3C2H_3-2 select the source of DCLK2 PLL values. The loading may be delayed a small but variable amount of time. Use SR15_5 to produce an immediate load.

Bit 2 DOS - DCLK Output Select
0 = Output controller 1 DCLK if SR15_3 =1
1 = Output controller 2 DCLK if SR15_3 =1

The clock (which clock depends on SR30_4-3) is output on the LCLK pin.

Bit 3 TB1 - PLL Test Bit 1
0 = Test DCLK1 if SR14_3 =0 or test MCLK if SR14_3 =1
1 = Test DCLK2 if SR14_3 =0 or reserved if SR14_3 =1

This bit is effective when SR14_2 =1 and is used for S3 test purposes only

Bit 4 D2B2 - Divide Controller 2 Dot Clock by 2
0 = Controller 2 dot clock is not divided by 2
1 = Divide Controller 2 dot clock by 2

This bit must be set to 1 if Controller 2 is used for clock doubled DAC operation (CR67_7-4= 0001b). Note that clock doubled mode is possible for CRT display only.

Bit 5 D2RC - Select DCLK2 PLL Reference Clock
0 = DCLK2 PLL reference clock comes from XIN input
1 = DCLK2 PLL reference clock comes from EDCLK2 input

Bit 6 IC2D - Invert Controller 2 Clock Doubled Dot Clock
0 = Controller 2 dot clock used for clock doubled mode is not inverted
1 = Controller 2 dot clock used for clock doubled mode is inverted

This bit affects Controller 2 dot clock that supplies the 2X clock in clock doubled DAC operation (CR67_7-4 = 0001b). This bit has no effect when Controller 2 is not in clock doubled mode.

Bit 7 ED2S - External DCLK2 Select
0 = DCLK2 is generated by internal PLL
1 = DCLK2 is input on EDCLK2 pin and driven by an external clock oscillator

This function can also be enabled when CR37_3 = 0.

Extended Sequencer D Register (SRD)

Read/Write Address: 3C5H, Index 0DH
Power-On Default: 00H

This register provides feature connector control and also provides independent control of the HSYNC and VSYNC signals, therefore supporting the VESA DPMS (Display Power Management Control) standard.

7	6	5	4	3	2	1	0
VSY-CTL		HSY-CTL					LPB
1	0	1	0	FLD	R	R	EN

Bit 0 LPBEN - LPBEN Pin Control
0 = LPBEN pin is held at logic 0
1 = LPBEN pin is held at logic 1

Bits 2–1 Reserved

Bit 3 FLD - Force LPB Disable
0 = LPB function can be enabled via MMFF00_0 = 1
1 = LPB function is disabled regardless of setting of MMFF00_1

Bits 5–4 HSY-CTL - HSYNC Control
00 = Normal operation
01 = HSYNC = 0
10 = HSYNC = 1
11 = Reserved

Bits 7–6 VSY-CTL - VSYNC Control
00 = Normal operation
01 = VSYNC = 0
10 = VSYNC = 1
11 = Reserved

Enhanced Mode DCLK2 Value Low Register (SRE)

Read/Write Address: 3C5H, Index 0EH
Power-On Default: Undefined

When DCLK2 is selected as the Controller 1 dot clock, SRE, SRF and SR29_4-2 are used as the source of the DCLK2 PLL parameter values only when 3C2H_3-2 = 11b (enhanced modes). When DCLK2 is selected as the Controller 2 dot clock, SRE, SRF and SR29_4-2 are always used. Loading of new values occurs when either SRB_1 is set to 1 or SR15_5 is programmed to 1 and then 0. Software must wait at least 100 µs after re-programming PLL values before further programming.

7	6	5	4	3	2	1	0
PLL R VALUE		PLL N-DIVIDER VALUE					

Bits 5-0 PLL N-DIVIDER VALUE

7-bit Value = the binary equivalent of the integer (1-127) divider used to scale the input to the DCLK PLL. Bit 6 of this value is SR29_4. See Section 8.

Bits 7-6 PLL R VALUE
000 = frequency divider of 1
001 = frequency divider of 2
010 = frequency divider of 4
011 = frequency divider of 8
100 = frequency divider of 16

The high order bit of this value is SR29_2. See Section 8 for a detailed explanation.

Enhanced Mode DCLK2 Value High Register (SRF)

Read/Write Address: 3C5H, Index 0FH
Power-On Default: Undefined

When DCLK2 is selected as the Controller 1 dot clock, SRE, SRF and SR29_3-2 are used as the source of the DCLK2 PLL parameter values only when 3C2H_4-2 = 11b (enhanced modes). When DCLK2 is selected as the Controller 2 dot clock, SRE, SRF and SR29_4-2 are always used. Loading of new values occurs when either SRB_1 is set to 1 or SR15_5 is programmed to 1 and then 0. Software must wait at least 100 µs after re-programming PLL values before further programming.

7	6	5	4	3	2	1	0
PLL M-DIVIDER VALUE							

Bits 7-0 PLL M- DIVIDER VALUE

9-bit Value = the binary coding of the integer (1-511) divider used in the feedback loop of the DCLK PLL. Bit 8 of this value is SR29_3. See Section 8 for a detailed explanation.

MCLK Value Low Register (SR10)

Read/Write Address: 3C5H, Index 10H
Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR11 generate an MCLK value of 45 MHz. (A read after reset returns 00H.) All other MCLK values must be specified by programming of SR10 and SR11. Loading of a new value is enabled by either bit 0 or bit 5 of SR15. Software must wait at least 100 μs after re-programming PLL values before further programming.

7	6	5	4	3	2	1	0
R	PLL R VALUE		PLL N-DIVIDER VALUE				

Bits 4-0 PLL N-DIVIDER VALUE

Value = the binary equivalent of the integer (1-31) divider used to scale the input to the MCLK PLL. See Section 8 for a detailed explanation.

Bits 6-5 PLL R VALUE
00 = frequency divider of 1
01 = frequency divider of 2
10 = frequency divider of 4
11 = frequency divider of 8

See Section 8 for a detailed explanation.

Bit 7 Reserved

MCLK Value High Register (SR11)

Read/Write Address: 3C5H, Index 11H
Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR10 generate an MCLK value of 45 MHz. (A read after reset returns 00H.) All other MCLK values must be specified by programming of SR10 and SR11. Loading of a new value is enabled by either bit 0 or bit 5 of SR15. Software must wait at least 100 μs after re-programming PLL values before further programming.

7	6	5	4	3	2	1	0
R	PLL M-DIVIDER VALUE						

Bits 6-0 PLL M-DIVIDER VALUE

Value = the binary equivalent of the integer (1-127) divider used in the feedback loop of the MCLK PLL. See Section 8 for a detailed explanation.

Bit 7 Reserved

Enhanced Mode DCLK1 Value Low Register (SR12)

Read/Write Address: 3C5H, Index 12H
Power-On Default: Undefined

When DCLK1 is selected as the Controller 1 dot clock and not selected as the Controller 2 dot clock, SR12, SR13 and SR29_0 are used as the source of the DCLK PLL parameter values only when 3C2H_3-2 = 11b (enhanced modes). When DCLK1 is selected as the Controller 2 dot clock, SRE, SRF and SR29_0 are always used. Loading of new values occurs when either SRB_1 is set to 1 or SR15_5 is programmed to 1 and then 0. Software must wait at least 100 μs after re-programming PLL values before further programming.

7	6	5	4	3	2	1	0
PLL R VALUE		R	PLL N-DIVIDER VALUE				

Bits 4-0 PLL N-DIVIDER VALUE

Value = the binary equivalent of the integer (1-31) divider used to scale the input to the DCLK1 PLL. See Section 8 for a detailed explanation.

Bit 5 Reserved

Bits 7-6 PLL R VALUE
000 = frequency divider of 1
001 = frequency divider of 2
010 = frequency divider of 4
011 = frequency divider of 8
100 = frequency divider of 16

The high order bit of this value is SR29_0. See Section 8 for a detailed explanation.

Enhanced Mode DCLK1 Value High Register (SR13)

Read/Write Address: 3C5H, Index 13H
Power-On Default: Undefined

When DCLK1 is selected as the Controller 1 dot clock and not selected as the Controller 2 dot clock, SR12, SR13 and SR29_0 are used as the source of the DCLK PLL parameter values only when 3C2H_3-2 = 11b (enhanced modes). When DCLK1 is selected as the Controller 2 dot clock, SRE, SRF and SR29_0 are always used. Loading of new values occurs when either SRB_1 is set to 1 or SR15_5 is programmed to 1 and then 0. Software must wait at least 100 μs after re-programming PLL values before further programming.

7	6	5	4	3	2	1	0
R	PLL M-DIVIDER VALUE						

Bits 6-0 PLL M- DIVIDER VALUE

Value = the binary equivalent of the integer (1-255) divider used in the feedback loop of the DCLK1 PLL. See Section 8 for a detailed explanation.

Bit 7 Reserved

Clock Synthesizer Control 1 Register (SR14)

Read/Write Address: 3C5H, Index 14H
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT DCLK	EXT MCLK	LTS	CLR CNT	CLK TEST	EN CNT	MPLL PD	D1 PD

Bit 0 D1 PD - Power down DCLK1 PLL
0 = DCLK1 PLL powered
1 = DCLK1 PLL powered down

This bit is used for S3 test purposes only.

Bit 1 MPLL PD - Power down MCLK PLL
0 = MCLK PLL powered
1 = MCLK PLL powered down

This bit is used for S3 test purposes only.

Bit 2 EN CNT - Enable Clock Synthesizer Counters
0 = Clock synthesizer counters disabled
1 = Clock synthesizer counters enabled

See Section 8.4 for a description of the clock testing procedure.

Bit 3 CLK TEST - Clock Test
0 = Test DCLK1 if SRB_3 = 0 or test DCLK2 if SRB_3 = 1
1 = Test MCLK if SRB_3 = 0 or reserved if SRB_3 = 1

If DCLK1 or 2 is selected, ensure that 3C2H_3-2 = 11b. This bit is effective when SR14_2 = 1.

Bit 4 CLR CNT - Clear Clock Synthesizer Counter
0 = No effect
1 = Clear the clock synthesizer counter

Bit 5 LTS - LPBEN Pin Tri-state
0 = LPBEN pin has normal function
1 = LPBEN pin is tri-stated

Setting this bit to 1 allows pin N1 to act as an input. This is enabled by setting bit 6 of this register to 1.

Bit 6 EXT MCLK - External MCLK Select
0 = MCLK provided by internal PLL
1 = MCLK is input on LPBEN pin and driven by an external oscillator. This function can also be enabled when CR36_1 = 0 or when CR37_3 = 0.

An external MCLK is only used for S3 test purposes.

Bit 7 EXT DCLK - External DCLK1 Select
0 = DCLK1 provided by internal PLL
1 = DCLK1 is input on XIN pin. This function can also be enabled when CR37_3 = 0.

An external DCLK1 is only used for S3 test purposes.

Clock Synthesizer Control 2 Register (SR15)

Read/Write Address: 3C5H, Index 15H
Power-On Default: 00H

7	6	5	4	3	2	1	0
1 CYC MWR	DCLK INV	CLK LOAD	D1/2	DCLK OUT	MCLK OUT	DRFQ EN	MFRQ EN

Bit 0 MFRQ EN - Enable New MCLK Frequency Load
0 = Register bit clear
1 = Load new MCLK frequency

When new MCLK PLL values are programmed, this bit is set to 1 to load these values in the PLL. The loading may be delayed a small but variable amount of time. This bit should be cleared to 0 after loading to prevent repeated loading. Alternately, use bit 5 of this register to produce an immediate load.

Bit 1 DFRQ EN - Enable new DCLK1 Frequency Load
0 = Register bit clear
1 = Load new DCLK1 frequency

When new DCLK1 PLL values are programmed, this bit is set to 1 to load these values in the PLL. 3C2H_3-2 select the source of the DCLK1 PLL values. The loading may be delayed a small but variable amount of time. Use bit 5 of this register to produce an immediate load.

Bit 2 MCLK OUT - Output Internally Generated MCLK
0 = $\overline{\text{STWR}}$/GOP0 pin has its normal function
1 = $\overline{\text{STWR}}$/GOP0 pin outputs the internally generated MCLK if SR1A_4 = 1

This is used only for S3 testing.

Bit 3 DCLK OUT - Output Internally Generated DCLK
0 = LCLK pin has its normal function
1 = LCLK pin outputs DCLK1 or DCLK2, depending on setting of SRB_2

This is used only for S3 testing.

Bit 4 D1/2 - Divide Controller 1 DCLK by 2
0 = Controller 1 DCLK unchanged
1 = Controller 1 DCLK divided by 2

Bit 5 CLK LOAD - MCLK, DCLK Load
0 = Clock loading is controlled by bits 0 and 1 of this register
1 = Load MCLK, DCLK1 PLL and DCLK2 PLL values immediately

To produce an immediate MCLK and DCLK load, program this bit to 1 and then to 0. 3C2H_3-2 select the source of the DCLK PLL values. This register must never be left set to 1.

Bit 6 DCLK INV - Invert DCLK
0 = DCLK1 unchanged
1 = Invert DCLK1

This bit affects the Controller 1 dot clock that supplies the 2X clock in clock doubled DAC mode (CR67_7-4 = 0001b). It has no effect when Controller 1 is not in clock doubled mode.

Bit 7 1 CYC MWR - Enable 1 cycle Memory Write
0 = 2 MCLK memory write
1 = 1 MCLK memory write

This bit should be set to 1 only in Enhanced mode. This allows 1-cycle CPU writes to memory. CR76_0 and this bit must always be set to the same value.

CLKSYN Test High Register (SR16)

Read Only Address: 3C5H, Index 16H
Power-On Default: 00H

7	6	5	4	3	2	1	0
CLOCK TEST RESULTS HIGH BYTE							

Bits 7-0 CLOCK TEST RESULTS HIGH BYTE

See Section 8.4 for a description of how to use this register.

CLKSYN Test Low Register (SR17)

Read Only Address: 3C5H, Index 17H
Power-On Default: 00H

7	6	5	4	3	2	1	0
CLOCK TEST RESULTS LOW BYTE							

Bits 7-0 CLOCK TEST RESULTS LOW BYTE

See Section 8.4 for a description of how to use this register.

DAC/CLKSYN Control Register (SR18)

Read/Write Address: 3C5H, Index 18H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R=0	CLUT WR	DAC PD	TST RED	TST GRN	TST BLUE	TST RST	TST EN

Bit 0 TST EN - Enable Signature Test Counter
0 = DAC signature test counter disabled
1 = DAC signature test counter enabled

Bit 1 TST RST - Reset Signature Test Counter
0 = No effect
1 = Reset the DAC signature test counter

Bit 2 TST BLUE - Test Blue Data
0 = No effect
1 = Place blue data on internal data bus

The blue signature data is read via CR6E.

Bit 3 TST GRN - Test Green Data
0 = No effect
1 = Place green data on internal data bus

The green signature data is read via CR6E.

Bit 4 TST RED - Test Red Data
0 = No effect
1 = Place red data on internal data bus

The red signature data is read via CR6E.

Bit 5 DAC PD - DAC Power-down
0 = DAC powered up unless SR20_0 = 1
1 = DAC powered down

When the DAC is powered down, the DAC memory retains its data. Software should set this bit when only a flat panel (no CRT) is being driven.

Bit 6 LUT WR - CLUT Write Cycle Control
0 = 2 DCLK CLUT write cycle (default)
1 = 1 DCLK CLUT write cycle

Bit 7 Reserved = 0

TV DAC Control Register (SR19)

Read/Write Address: 3C5H, Index 19H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	TPD	ETS	TTM	R	R	R

Bits 2-0 Reserved

Bit 3 TTM - TV DAC Test Mode
0 = Normal operation
1 = TV DAC test mode enabled

This bit is used only for S3 testing.

Bit 4 ETS - Enable TV DAC Sense
0 = TV DAC sense circuit is powered down
1 = Enable TV DAC sense circuit

SR79 is programmed with a value. This value is driven to the DAC and converted to the AY output to be used by the $\overline{\text{SENSE}}$ circuit. Similarly, SR7A is programmed with a value. This value is driven to the DAC and converted to the AC output to be used by the $\overline{\text{SENSE}}$ circuit. The Y and C sense results can be read from SR1B_1 and SR1B_2 respectively. CR3D_0 must be set to 1 to enable AY and AC output.

Bit 5 TPD - TV DAC Power Down
0 = TV DAC powered
1 = TV DAC powered down

Setting this bit also powers down the TV DAC sense circuitry.

Bits 7-6 Reserved

Extended Sequencer 1A Register (SR1A)

Read/Write Address: 3C5H, Index 1AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
TVO	PDIO	R	S/G	FCTS		FCTM	FTEN

Bit 0 FTEN - Filter Capacitor Test Enable
0 = Disable filter capacitor test
1 = Enable filter capacitor test

The filter capacitor test is for use only by S3.

Bit 1 FCTM - Filter Capacitor Test Mode
0 = Leakage measurement test
1 = Voltage measurement test

Bits 3-2 FCTS - Filter Capacitor Test Select
00 = Filter capacitor test for DCLK1 PLL
01 = Filter capacitor test for MCLK PLL
10 = Filter capacitor test for DCLK2 PLL
11 = Reserved

Bit 4 S/G- STWR/GOP0 Select
0 = STWR/GOP0 pin functions as GOP0
1 = STWR/GOP0 pin functions as $\overline{\text{STWR}}$

Bit 5 Reserved

Bit 6 PDIO - Power Down Internal Oscillator
0 = Disable internal latch on XIN input. This setting must be used if the XIN input is driven when both MCLK AND DCLK1 PLLs are powered down AND either DCLK2 is powered down or SRB_5 = 1.
1 = Enable internal latch for the same conditions as the = 0 value except that the XIN input is not being driven when it is not being used

Bit 7 TVO - TV DAC Output Level
0 = TV DAC output level is approximately 43 mA
1 = TV DAC output level is approximately 34 mA

This bit should normally never be set to 1.

Extended Sequencer 1B Register (SR1B)

See Bit Descriptions Address: 3C5H, Index 1BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
FC1D	R	R	R	R	CS	YS	R

Bit 0 Reserved

Bit 1 YS - TV DAC Y Sense (Read Only)

This bit reflects the state of the Y sense circuit when SR19_4 = 1.

Bit 2 CS - TV DAC C Sense (Read Only)

This bit reflects the state of the C sense circuit when SR19_4 = 1.

Bits 6-3 Reserved

Bit 7 FC1D - Force Controller 1 DCLK Source
0 = Controller 1 dot clock PLL parameter source is determined by the settings of SR30_3, SR30_4 and 3C2H_3-2
1 = Controller 1 dot clock PLL parameter source is always SR12/SR13 if DCLK1 is driving Controller 1 and SRE/SRF if DCLK2 is driving Controller 1

Extended Sequencer 1C Register (SR1C)

Read/Write Address: 3C5H, Index 1CH
Power-On Default: 00H

All non-reserved bits in this register should be programmed to 1 by the BIOS during reset.

7	6	5	4	3	2	1	0
LSU	LSB	LP	TVSU	TVSB	TVP	C2D	C1D

Bit 0 C1D - Controller 1 DCLK Control
0 = Controller 1 DCLK going to the Streams Processor can be divided by 2 when SR1_3 or SR15_4 is set to 1 in non-flat panel modes
1 = Controller 1 DCLK going to the Streams Processor will not be divided by 2 when SR1_3 or SR15_4 is set to 1 in non-flat panel modes

Setting this bit to 1 is required when Controller 1 is driving the TV DAC.

Bit 1 C2D - Controller 2 DCLK Control
0 = Controller 2 DCLK going to the Streams Processor can be divided by 2 when SR1_3 or SR15_4 is set to 1 in non-flat panel modes
1 = Controller 2 DCLK going to the Streams Processor will not be divided by 2 when SR1_3 or SR15_4 is set to 1 in non-flat panel modes

Setting this bit to 1 is required when Controller 2 is driving the TV DAC.

Bit 2 TVP - TV Encoder Powerdown Enable
0 = TV Encoder clock is not turned off when TV Encoder is disabled
1 = TV Encoder clock is turned off when TV Encoder is disabled

Bit 3 TVSB - TV Encoder Standby Enable
0 = TV Encoder clock is not turned off in Standby mode
1 = TV Encoder clock is turned off in Standby mode

Bit 4 TVSU - TV Encoder Suspend Enable
0 = TV Encoder clock is not turned off in Suspend mode
1 = TV Encoder clock is turned off in Suspend mode

Bit 5 LP - LPB Powerdown Enable
0 = LPB LCLK is not turned off when LPB is disabled
1 = LPB LCLK is turned off when LPB is disabled

Bit 6 LSB - LPB Standby Enable
0 = LPB LCLK is not turned off in Standby mode
1 = LPB LCLK is turned off in Standby mode

Bit 7 LSU - LPB Suspend Enable
0 = LPB LCLK is not turned off in Suspend mode
1 = LPB LCLK is turned off in Suspend mode

Extended Sequencer 1D Register (SR1D)

Read/Write Address: 3C5H, Index 1DH
Power-On Default: 00H

This register controls the powerdown for Stream Processor (SP) dot clock (DCLK). These bits control powerdown of DCLK used on portion of stream processor logic that can be turned off when the Stream Processor is disabled.

All non-reserved bits in this register should be programmed to 1 by the BIOS during reset.

7	6	5	4	3	2	1	0
R	R	SSU1	SSB1	SP1	SPV	SPH	R

Bit 0 Reserved

Bit 1 SPH - Stream Processor Horizontal Powerdown Enable
0= SP DCLK is not turned off in pixels where there is no secondary stream within lines where there is secondary stream
1 = SP DCLK is turned off in pixels where there is no secondary stream within lines where there is secondary stream

Bit 2 SPV - Stream Processor Vertical Powerdown Enable
0= SP DCLK is not turned off in lines where there is no secondary stream
1 = SP DCLK is turned off in lines where there is no secondary stream

Bit 3 SP1 - Stream Processor Powerdown Enable
0 = SP DCLK is not turned off when SP is disabled
1 = SP DCLK is turned off when SP is disabled

Bit 4 SSB1 - Stream Processor Standby Enable
0 = SP DCLK is not turned off in Standby mode
1 = SP DCLK is turned off in Standby mode

Bit 5 SSU1 - Stream Processor Suspend Enable
0 = SP DCLK is not turned off in Suspend mode
1 = SP DCLK is turned off in Suspend mode

Bit 7-6 Reserved

Power Management 5 Register (SR1E)

Read/Write Address: 3C5H, Index 1EH
Power-On Default: 00H

All non-reserved bits in this register should be programmed to 1 by the BIOS during reset.

7	6	5	4	3	2	1	0
BSE	R	R	C2SU	C2SB	C2PD	R	C1PD

Bit 0 C1PD - Controller 1 Powerdown Enable
0 = Controller 1 DCLK is not turned off when Controller 1 is not enabled
1 = Controller 1 DCLK is turned off when Controller 1 is not enabled

Controller 1 is enabled when SR31_1 = 0 or when SR31_2 = 0 and SR31_4 = 1)

Bit 1 Reserved

Bit 2 C2PD - Controller 2 Power Down Enable
0 = Controller 2 DCLK is not turned off when Controller 2 is not enabled
1 = Controller 2 DCLK is turned off when Controller 2 is not enabled

Controller 2 is enabled when SR31_1 = 1 or when SR31_2 = 1 and SR31_4 = 1)

Bit 3 C2SB - Controller 2 Power Down During Standby
0 = Controller 2 is not powered down during Standby
1 = Controller 2 is powered down during Standby

Bit 4 C2SU - Controller 2 Power Down During Suspend
0 = Controller 2 is not powered down during Suspend
1 = Controller 2 is powered down during Suspend

Bits 6-5 Reserved

Bit 7 BSE - Bus Interface Suspend Enable
0 = Bus interface SCLK is not turned off during Suspend
1 = Bus interface SCLK is turned off during Suspend

Extended Sequencer 1F Register (SR1F)

Read/Write Address: 3C5H, Index 1FH
Power-On Default: 00H

All non-reserved bits in this register should be programmed to 1 by the BIOS during reset.

7	6	5	4	3	2	1	0
PFIE	R	C5VT	M5VT	R	R	N3D	3DSE

Bit 0 3DSE - S3D Engine Suspend Enable
0 = S3d MCLK is not turned off in Suspend mode
1 = S3d MCLK is turned off in Suspend mode

Bit 1 N3D - Non-S3D MCLK Suspend Enable
0 = MCLK outside S3d engine is not turned off in Suspend mode
1 = MCLK outside S3d engine is turned off in Suspend mode

Bits 3-2 Reserved

Bit 4 M5VT - Memory Interface 5V Tolerant Control
0 = Memory interface is 5V tolerant
1 = Memory interface is not 5V tolerant

This bit should be initialized by the BIOS to the correct state as soon as possible during boot up. If the 5V tolerant interface is programmed, VDDMEM5 must be set to 5V and each pad consumes a static current of approximately 25 microamps. If this bit is set to 1, VDDMEM5 must be set to 3.3V.

Bit 5 C5VT - CPU Interface 5V Tolerant Control
0 = CPU interface is 5V tolerant
1 = CPU interface is not 5V tolerant

This bit should be initialized by the BIOS to the correct state as soon as possible during boot up. If the 5V tolerant interface is programmed, VDDSYS5 must be set to 5V and each pad consumes a static current of approximately 25 microamps. If this bit is set to 1, VDDSYS5 must be set to 3.3V.

Bit 6 L5VT - LPB/CRT Interface 5V Tolerant Control
0 = LPB/CRT interface is 5V tolerant
1 = LPB/CRT interface is not 5V tolerant

This bit should be initialized by the BIOS to the correct state as soon as possible during boot up. If the 5V tolerant interface is programmed, VDDLPB5 must be set to 5V and each pad consumes a static current of approximately 25 microamps. If this bit is set to 1, VDDLPB5 must be set to 3.3V.

Bit 7 FPU - Flat Panel Interface Pull-Up Control
0 = Normal pull-up strength for the flat panel interface
1 = Higher pull-up strength (faster rise time) for the flat panel interface

If this bit is set to 1, each pad consumes a static current of approximately 10 microamps. Therefore, this bit should be used only if required and should always be cleared to 0 before going into Standby or Suspend.

Extended Sequencer 20 Register (SR20)

Read/Write Address: 3C5H, Index 20H
Power-On Default: 00H

7	6	5	4	3	2	1	0
PSE	TSUE	TSTE	MPSE	D1SE	DSUE	DSBE	D2SE

Bit 0 D2SE - DCLK2 PLL Suspend Enable
0 = DCLK2 is not turned off in Suspend mode
1 = DCLK2 is turned off in Suspend mode

Bit 1 DSBE - CRT DAC Standby Enable
0 = CRT DAC is not turned off in Standby mode
1 = CRT DAC is turned off in Standby mode

Bit 2 DSUE - CRT DAC Suspend Enable
0 = CRT DAC is not turned off in Suspend mode
1 = CRT DAC is turned off in Suspend mode

Bit 3 D1SE - DCLK1 PLL Suspend Enable
0 = DCLK1 PLL is not turned off in Suspend mode
1 = DCLK1 PLL is turned off in Suspend mode

Bit 4 MPSE - MCLK PLL Suspend Enable
0 = MCLK PLL is not turned off in Suspend mode
1 = MCLK PLL is turned off in Suspend mode

Bit 5 TSTE - TV DAC Standby Enable
0 = TV DAC is not turned off in Standby mode
1 = TV DAC is turned off in Standby mode

Bit 6 TSUE- CRT DAC Suspend Enable
0 = CRT DAC is not turned off in Suspend mode
1 = CRT DAC is turned off in Suspend mode

Bit 7 PSE - Pads Suspend Enable
0 = Suspend mode has no effect on pads
1 = Suspend mode puts the pads in Suspend configuration

Extended Sequencer 21 Register (SR21)

Read/Write Address: 3C5H, Index 21H
Power-On Default: 00H

7	6	5	4	3	2	1	0
C2LE	C2LS	C2LP	LUT2	C1LE	C1LS	MS	LUT1

Bit 0 LUT1 - Disable CLUT1
0 = CLUT1 enabled
1 = CLUT1 disabled (powered down)

Bit 1 MS - Disable Monitor Sense
0 = Monitor sense circuit enabled
1 = Monitor sense circuit disabled (powered down)

Bit 2 C1LS - Controller 1 CLUT Standby Enable
0 = Controller 1 CLUT is not powered down in Standby mode
1 = Controller 1 CLUT is powered down in Standby mode

The BIOS must program this bit to 1 after each reset.

Bit 3 C1LE - Controller 1 CLUT Suspend Enable
0 = Controller 1 CLUT is not powered down in Suspend mode
1 = Controller 1 CLUT is powered down in Suspend mode

The BIOS must program this bit to 1 after each reset.

Bit 4 LUT2 - Disable CLUT2
0 = CLUT2 enabled
1 = CLUT2 disabled (powered down)

Bit 5 C2LP - Controller 2 CLUT Powerdown Enable
0 = Controller 2 CLUT is not powered down when Controller 2 is not enabled
1 = Controller 2 CLUT is powered down when Controller 2 is not enabled

The BIOS must program this bit to 1 after each reset.

Bit 6 C2LS - Controller 2 CLUT Standby Enable
0 = Controller 2 CLUT is not powered down in Standby mode
1 = Controller 2 CLUT is powered down in Standby mode

The BIOS must program this bit to 1 after each reset.

Bit 7 C2LE - Controller 2 CLUT Suspend Enable
0 = Controller 2 CLUT is not powered down in Suspend mode
1 = Controller 2 CLUT is powered down in Suspend mode

The BIOS must program this bit to 1 after each reset.

VGA Clock 1 Value Low Register (SR22)

Read/Write Address: 3C5H, Index 22H
Power-On Default: See description below

SR22 and SR23 are selected as the source of the Controller 1 DCLK PLL parameter values (either DCLK1 or DCLK2) when 3C2H_3-2 = 00b unless the Controller 1 DCLK is also driving Controller 2. See the definition for 3C32H_3-2. The power-on default value for this register in conjunction with the power-on default value for SR23 generate a DCLK value of 25.175 MHz. Loading of new values occurs when either SR15_1 is set to 1 or SR15_5 is programmed to 1 and then 0. Software must wait at least 100 µs after re-programming PLL values before further programming.

7	6	5	4	3	2	1	0
PLL R VALUE		R	PLL N-DIVIDER VALUE				

Bits 4-0 N-DIVIDER VALUE

Value = the binary equivalent of the integer (1-31) divider used to scale the input to the DCLK PLL. See Section 8 for a detailed explanation.

Bit 5 Reserved

Bits 7-6 PLL R VALUE
00 = frequency divider of 1
01 = frequency divider of 2
10 = frequency divider of 4
11 = frequency divider of 8

See Section 8 for a detailed explanation.

VGA Clock 1 Value High Register (SR23)

Read/Write Address: 3C5H, Index 23H
Power-On Default: See description below.

SR22 and SR23 are selected as the source of the Controller 1 DCLK PLL parameter values (either DCLK1 or DCLK2) when 3C2H_3-2 = 00b unless the Controller 1 DCLK is also driving Controller 2. See the definition for 3C32H_3-2. The power-on default value for this register in conjunction with the power-on default value for SR22 generate a DCLK value of 25.175 MHz. Loading of new values occurs when either SR15_1 is set to 1 or SR15_5 is programmed to 1 and then 0. Software must wait at least 100 μs after re-programming PLL values before further programming.

7	6	5	4	3	2	1	0
R	PLL M-DIVIDER VALUE						

Bits 6-0 PLL M- DIVIDER VALUE

Value = the binary equivalent of the integer (1-127) divider used in the feedback loop of the DCLK PLL. See Section 8 for a detailed explanation.

Bit 7 Reserved

VGA Clock 2 Value Low Register (SR24)

Read/Write Address: 3C5H, Index 24H
Power-On Default: See description below

SR24 and SR25 are selected as the source of the Controller 1 DCLK PLL parameter values (either DCLK1 or DCLK2) when 3C2H_3-2 = 00b unless the Controller 1 DCLK is also driving Controller 2. See the definition for 3C32H_3-2. The power-on default value for this register in conjunction with the power-on default value for SR25 generate a DCLK value of 28.322 MHz. Loading of new values occurs when either SR15_1 is set to 1 or SR15_5 is programmed to 1 and then 0. Software must wait at least 100 μs after re-programming PLL values before further programming.

7	6	5	4	3	2	1	0
PLL R VALUE		R	PLL N-DIVIDER VALUE				

Bits 4-0 N-DIVIDER VALUE

Value = the binary equivalent of the integer (1-31) divider used to scale the input to the DCLK PLL. See Section 8 for a detailed explanation.

Bit 5 Reserved

Bits 7-6 PLL R VALUE
00 = frequency divider of 1
01 = frequency divider of 2
10 = frequency divider of 4
11 = frequency divider of 8

See Section 8 for a detailed explanation.

VGA Clock 2 Value High Register (SR25)

Read/Write Address: 3C5H, Index 25H
Power-On Default: See description below.

SR24 and SR25 are selected as the source of the Controller 1 DCLK PLL parameter values (either DCLK1 or DCLK2) when 3C2H_3-2 = 00b unless the Controller 1 DCLK is also driving Controller 2. See the definition for 3C32H_3-2. The power-on default value for this register in conjunction with the power-on default value for SR24 generate a DCLK value of 28.322 MHz. Loading of new values occurs when either SR15_1 is set to 1 or SR15_5 is programmed to 1 and then 0. Software must wait at least 100 μs after re-programming PLL values before further programming.

7	6	5	4	3	2	1	0
R	PLL M-DIVIDER VALUE						

Bits 6-0 PLL M- DIVIDER VALUE

Value = the binary equivalent of the integer (1-127) divider used in the feedback loop of the DCLK PLL. See Section 8 for a detailed explanation.

Bit 7 Reserved

Paired Register Read/Write Select Register (SR26)

Read/Write Address: 3C5H, Index 26H
Power-On Default: 00H

7	6	5	4	3	2	1	0
VISS	L1PD	R	R	DC1W	EC2W	DR	DSR

Bit 0 DSR - Disable Selected Controller 1 Reads
0 = Data for all paired register reads comes from the Controller 1 registers
1 = Reads of CR0-CR7, CR10-12, CR15-16 from Controller 1 are disabled. Read data is provided from the corresponding paired registers in Controller 2

This bit is only effective if bit 1 of this register is cleared to 0.

Bit 1 DR - Disable Controller 1 Reads
0 = Data for all paired register reads comes from the Controller 1 registers
1 = Reads of all paired controller 1 registers are disabled. Read data is provided from the corresponding paired registers in Controller 2

Setting this bit to 1 overrides the setting of bit 0 of this register.

Bit 2 EC2W - Enable Controller 2 Writes
0 = Writes to controller 2 registers are disabled
1 = Writes to controller 2 registers are enabled

Note that by default, writes to Controller 1 registers (controlled by bit 3 of this register) are enabled and writes to Controller 2 registers are disabled. Software can selectively write to only Controller 1 registers, only Controller 2 registers or to both with one write (mirroring) by enabling writes to both.

Bit 3 DC1W - Disable Controller 1 Writes
0 = Writes to Controller 1 registers are enabled
1 = Writes to Controller 1 registers are disabled

See the note for bit 2 of this register.

Note: If this bit is set to 1, any subsequent writes to any SR register will be directed to SR26 (the index is locked). Therefore, no writes to SR registers (except SR26) should be made if this bit is set to 1.

Bits 5-4 Reserved

Bit 6 L1PD - CLUT1 Power Down
0 = CLUT1 is powered down during blank time
1 = CLUT1 is not powered down during blank time

Powering down CLUT1 during blank time when TV is enabled will cause a vertical stripe artifact. Therefore, this bit must be set to 1 when TV is enabled.

Bit 7 VISS - Vertical Interrupt Source Select
0 = Vertical interrupt source is Controller 1
1 = Vertical interrupt source is Controller 2

DAC Current Control Register (SR27)

Read/Write Address: 3C5H, Index 27H
Power-On Default: 00H

7	6	5	4	3	2	1	0
DPD	TV DAC ADJUST			BPE	CRT DAC ADJUST		

Bits 2-0 CRT DAC ADJUST

These bits are used to adjust the gain of the CRT DAC.

Bit 3 BPE - $\overline{\text{BLANK}}$ Pedestal Enable
0 = Disable $\overline{\text{BLANK}}$ pedestal
1 = Enable $\overline{\text{BLANK}}$ pedestal

Bits 6-4 TV DAC ADJUST

These bits are used to adjust the gain of the TV DAC.

Bit 7 DPD - DAC Power Down
0 = CRT DAC powered down during blanking
1 = CRT DAC never powered down

PLL IREF Control Register (SR28)

Read/Write Address: 3C5H, Index 28H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	DCLK2 IFEF		DCLK1 IREF		MCLK IREF	

Bits 1-0 MCLK IREF

These bits adjust the IREF current of the MCLK PLL.

Bits 3-2 DCLK1 IREF

These bits adjust the IREF current of the DCLK1 PLL.

Bits 5-4 DCLK2 IREF

These bits adjust the IREF current of the DCLK2 PLL.

Bits 7-6 Reserved

DCLK PLL Value Overflow Register (SR29)

Read/Write Address: 3C5H, Index 29H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	D2N6	D2M2	D2R2	R	D1R2

Bit 0 D1R2 - DCLK1 PLL R Value Bit 2

See the description for SR12.

Bit 1 Reserved

Bit 2 D2R2 - DCLK2 PLL R Value Bit 2

See the description for SRE.

Bit 3 D2M2 - DCLK2 PLL M Value Bit 8

See the description for SRF.

Bit 4 D2N6 - DCLK2 PLL N Value Bit 6

See the description for SRE.

Bits 7-5 Reserved

Section 18: Extended CRTC Register Descriptions

All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, CR38 and/or CR39 must be loaded with a changed key pattern (see the register descriptions). The registers will remain unlocked until the key pattern is reset by altering a significant bit. If a register or bit is noted as paired, there are two identical registers or bits at that address, with access controlled via SR26. One register or bit is used by Controller 1 and the other for Controller 2.

In the following register descriptions, 'R' stands for reserved (write =0, read = undefined). See Appendix A for a table listing each register in this section and its page number.

CRT Test 1 Register (CTR22)

Read/Write Address: 3?5H, Index 22H
Power-On Default: 00H Paired

This register is accessible at Index 22H (instead of CR22) when CR39 = A5H.

7	6	5	4	3	2	1	0
TDD	R	R	R	R	R	R	R

Bits 6-0 Reserved

Bit 7 TDD - Test DAC Data
0 = Normal operation
1 = 24 bits of data are provided to the DAC by internal counters.

This bit must be set for the appropriate controller when either SR5F_0 = 1 (disabling Controller 1 frame buffer accesses) or SR5F_1 = 1 (disabling Controller 2 frame buffer accesses).

Synchronization 1 Register (CTR23)

Read/Write Address: 3?5H, Index 23H
Power-On Default: 00H

This register must be 00H before CTR26 is written. For this to be effective, A5H must first be programmed into CR39.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved

Synchronization 2 Register (CTR26)

Read/Write Address: 3?5H, Index 26H
Power-On Default: 00H

The BIOS must write 00H to this register upon each mode set (assuming CTR23 is at its default value of 00H). Drivers should write 00H to this register after writing 00H to CTR23 before enabling Streams Processor operation. For this to be effective, A5H must first be programmed into CR39.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved

Device ID High Register (CR2D)

Read Only Address: 3?5H, Index 2DH
Power-On Default: 8CH

This register should contain the same value as the upper byte of the PCI Device ID (Index 02H) register.

7	6	5	4	3	2	1	0
CHIP ID HIGH							

Bits 7–0 CHIP ID HIGH

value = 8CH (hardwired)

Device ID Low Register (CR2E)

Read Only Address: 3?5H, Index 2EH
Power-On Default: 01H

7	6	5	4	3	2	1	0
CHIP ID LOW							

Bits 7–0 CHIP ID LOW

value = 01H

Revision Register (CR2F)

Read Only Address: 3?5H, Index 2FH
Power-On Default: xxH

7	6	5	4	3	2	1	0
REVISION LEVEL							

Bits 7–0 REVISION LEVEL

This value will vary by chip revision.

Chip ID/REV Register (CR30)

Read Only Address: 3?5H, Index 30H
Power-On Default: E1H

When the software detects EH in the upper nibble of this register, it should then use CR2D, CR2E and CR2F for chip ID information.

7	6	5	4	3	2	1	0
CHIP ID				REVISION STATUS			

Bits 7–0 CHIP ID AND REVISION STATUS

Memory Configuration Register (CR31)

Read/Write Address: 3?5H, Index 31H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	HST DFF	R	R	ENH MAP	VGA 16B	SCRN 2.PG	EN CBA

Bit 0 EN CBA - Enable CPU Base Address Offset
0 = Address offset bits (CR6A_5-0) are disabled
1 = Address offset bits (CR6A_5-0) are enabled

Bit 1 SCRN 2.PG - Enable Two-Page Screen Image
0 = Normal Mode
1 = Enable 2K x 1K x 4 map image screen for 1024 × 768 or 800 x 600 screen resolution, or 2K x 512 x 8 map image screen for 640 x 480 screen resolution

Bit 2 VGA 16B - Enable VGA 16-bit Memory Bus Width
0 = 8-bit memory bus operation
1 = Enable 16-bit bus VGA memory read/writes

This is useful in VGA text modes when VGA graphics controller functions are typically not used.

Bit 3 ENH MAP - Use Enhanced Mode Memory Mapping
0 = Force IBM VGA mapping for memory accesses
1 = Force Enhanced Mode mappings

Setting this bit to 1 overrides the settings of bit 6 of CR14 and bit 3 of CR17 and causes the use of doubleword memory addressing mode. Also, the function of bits 3-2 of GR6 is overridden with a fixed 64K map at A0000H.

Note: This bit is forced to 1 for Controller 2 operation.

Bits 5–4 Reserved

Bit 6 HST DFF - Enable High Speed Text Display Font Fetch Mode
0 = Normal font access mode
1 = Enable high speed text display

Setting this bit to 1 is only required for DCLK rates greater than 40 MHz. See bit 5 of CR3A.

Bit 7 Reserved

Backward Compatibility 1 Register (CR32)

Read/Write Address: 3?5H, Index 32H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	VGA FXPG	R	INT EN	R	FCCH	R	R

Bits 1–0 Reserved

Bit 2 FCCH - Force Character Clock High
0 = Normal character clock
1 = Force horizontal timings to be based on undivided DCLK even if SR1_3 is set to 1 to divide DCLK by 2

Bit 3 Reserved

Bit 4 INT EN -Interrupt Enable
0 = All interrupt generation disabled
1 = Interrupt generation enabled

Bit 5 Reserved

Bit 6 VGA FXPG - Use Standard VGA Memory Wrapping
0 = Memory accesses extending past a 256K boundary do not wrap
1 = Memory accesses extending past a 256K boundary wrap at the boundary

The standard 256K VGA memory page always ends on a natural 256K boundary and accesses beyond this boundary will wrap. If the starting address is moved via bits 2-0 of CR69, the 256K page may not end on a 256K boundary and accesses past the boundary will not wrap. This is the case when this bit is cleared to 0. For standard VGA compatibility when the page base address is moved, this bit is set to 1 to cause wrapping at a 256K boundary.

Note: This bit is forced to 0 for Controller 2 operation.

Bit 7 Reserved

Backward Compatibility 2 Register (CR33)

Read/Write unless noted Address: 3?5H, Index 33H
Power-On Default: 00H

7	6	5	4	3	2	1	0
FFOE	LOCK PLTW	BDR SEL	LOCK DACW	VCLK= -DCK	VSA	DIS VDE	DMI

Bit 0 DMI - Display Mode Inactive (Read only)
0 = The controller is in the active display area
1 = The controller is not in the active display area

Note: This bit is paired. For Controller 1, this bit has the same functionality as 3?AH_0.

Bit 1 DIS VDE - Disable Vertical Display End Extension Bits Write Protection
0 = VDE protection enabled
1 = Disables the write protect setting of the bit 7 of CR11 on bits 1 and 6 of CR7

Bit 2 VSA - Vertical Sync Active (Read only)
0 = The controller is not in the vertical retrace area
1 = The controller is in the vertical retrace area

Note: This bit is paired. For Controller 1, this bit has the same functionality as 3?AH_3.

Bit 3 VCLK = -DCK - VCLK is Inverted DCLK
0 = VCLK is determined by other bit settings
1 = VCLK is forced to inverted DCLK

Note: This bit is paired.

Bit 4 LOCK DACW - Lock DAC Writes
0 = Enable writes to DAC registers
1 = Disable writes to DAC registers

Bit 5 BDR SEL - Blank/Border Select
0 = $\overline{\text{BLANK}}$ active time is defined by CR2 and CR3
1 = $\overline{\text{BLANK}}$ is active during entire display inactive period (no border)

Note: This bit is paired.

Bit 6 LOCK PLTW - Lock Palette/Border Color Registers
0 = Unlock Palette/Border Color registers
1 = Lock Palette/Border Color registers

Bit 7 FFOE - Flicker Filter Odd/Even Field Status (Read only)
0 = Current flicker filter field is even
1 = Current flicker filter field is odd

Note: This bit is paired.

Backward Compatibility 3 Register (CR34)

Read/Write Address: 3?5H, Index 34H
Power-On Default: 00H

7	6	5	4	3	2	1	0
LOCK CLKS	R	LOCK 8/9D	ENB SFF	R	PCI RET	PCI ABT	PCI SNP

Bit 0 PCI SNP - PCI DAC snoop method
0 = Handling of PCI master aborts and retries during DAC cycles controlled by bits 1 and 2 of this register
1 = PCI master aborts and retries are not handled during DAC cycles

Bit 1 PCI ABT - PCI master aborts during DAC cycles
0 = PCI master aborts handled during DAC cycles
1 = PCI master aborts not handled during DAC cycles

Bit 0 of this register must be cleared to 0 for this bit to be effective.

Bit 2 PCI RET - PCI retries during DAC cycles
0 = PCI retries handled during DAC cycles
1 = PCI retries not handled during DAC cycles

Bit 0 of this register must be cleared to 0 for this bit to be effective.

Bits 4-3 Reserved

Bit 5 LOCK 8/9D - Lock 8/9 Dots
0 = Bit 0 of SR1 is unlocked
1 = Bit 0 of SR1 is locked

This bit locks/unlocks selection of either an 8 dot or 9 dot character clock.

Bit 6 Reserved

Bit 7 LOCK CLKS - Lock Clock Select
0 = Bits 3-2 of 3C2H are unlocked
1 = Bits 3-2 of 3C2H are locked

This bit locks/unlocks selection of the the DCLK frequency.

CRT Register Lock Register (CR35)

Read/Write Address: 3?5H, Index 35H
Power-On Default: 00H Paired

7	6	5	4	3	2	1	0
LOCK CR12	LOCK CR1	LOCK HTMG	LOCK VTMG	R	R	R	R

Bits 3–0 Reserved

Bit 4 LOCK VTMG - Lock Vertical Timing Registers
0 = Vertical timing registers are unlocked
1 = The following vertical timing registers are locked:

CR6
CR7 (bits 7,5,3,2,0)
CR9 (bit 5)
CR10
CR11 (bits 3-0)
CR15
CR16

CR6, CR7 registers are also locked by bit 7 of the Vertical Retrace End register (CR11).

Note: This bit is paired.

Bit 5 LOCK HTMG - Lock Horizontal Timing Registers
0 = Horizontal timing registers are unlocked
1 = The following horizontal timing registers are locked:

CR0
CR2
CR3
CR4
CR5
CR17 (bit 2)

All these registers (except bit 2 of CR17) are also locked by bit 7 of the Vertical Retrace End register (CR11).

Note: This bit is paired.

Bit 6 LOCK CR1
0 = CR1 and 3C2H_6 unlocked
1 = CR1 and 3C2H_6 locked

Bit 7 LOCK CR12
0 = CR12 and 3C2H_7 unlocked
1 = CR12 and 3C2H_7 locked

Configuration 1 Register (CR36)

Read/Write Address: 3?5H, Index 36H
Power-On Default: Depends on Strapping

This register samples the reset state from PD bus pins [7:0]. These pins have internal pull-downs and their states are inverted during reset, so non-reserved register bits will default to 1 if the corresponding pin is not pulled up. Other configuration strapping bits are found in CR37 and CR68 and CR6F. This can be written only after A5H is written to CR39.

7	6	5	4	3	2	1	0
MEM SIZE		R	R	MEM TYPE		MCS	PI

Bit 0 PI - PCI Interrupt
0 = PCI register at offset 3DH reads 01H (INTA used as interrupt line)
1 = PCI register at offset 3DH reads 00H (no interrupt claimed)

Bit 1 MCS - Memory Clock Select
0 = Use external MCLK on LPBEN pin
1 = Use internal MCLK

The invert of this bit, the invert of CR37_3 and SR14_6 are all ORed.

Bit 3-2 MEM TYPE
00 = Reserved
01 = 1-cycle EDO
10 = Reserved
11 = SDRAM/SGRAM

Bits 5-4 Reserved

Bits 7-6 MEM SIZE
00 = Reserved
01 = 4 MBytes
10 = Reserved
11 = 2 MBytes

These PD bits should not be strapped, as they are overwritten by the BIOS after boot up.

Configuration 2 Register (CR37)

Read/Write Address: 3?5H, Index 37H
Power-On Default: Depends on Strapping

This register samples the reset state from PD bus pins [15:8]. These pins have internal pull-downs and their states are inverted during reset, so non-reserved register bits will default to 1 if the corresponding pin is not pulled up. Other configuration strapping bits are found in CR36, CR68 and CR6F. These bits can be written only after A5H is written to CR39.

7	6	5	4	3	2	1	0
PANEL TYPE				CS	SIDS	NTT	DIA

Bit 0 DIA - Disable I/O Access
0 = Disable I/O access
1 = I/O access can be enabled by setting PCI04_0 to 1

If I/O access is disabled, 3C3H_0 is forced to 1 (VGA enabled) and PCI04_0 is ignored.

Bit 1 NTT - NAND Tree Test
0 = NAND tree testing enabled (allows testing for bad solder connections. See Section 5.)
1 = Normal Operation

Bit 2 SIDS - Subsystem ID Source
0 = Read subsystem ID information from CR95-CR98
1 = Read subsystem ID information from BIOS ROM

Bit 3 CS - Clock Select
0 = Use external MCLK on LPBEN pin, external DCLK1 on XIN pin and external DCLK2 on EDCLK2 pin
1 = Use internal MCLK, DCLK1 and DCLK2

This is used for test purposes only.

Bit 4 Reserved

Bits 7-5 PANEL TYPE

OEMs can strap PD[15:13] to allow identification of up to 8 different panel types. The coding used is defined by each OEM.

Register Lock 1 Register (CR38)

Read/Write Address: 3?5H, Index 38H
Power-On Default: 00H

Loading 01xx10xx (e.g., 48H) into this register unlocks the extended CRTC registers from CR2D through CR3F for read/writes. (x = don't care)

7	6	5	4	3	2	1	0
= 0	= 1			= 1	= 0		

Register Lock 2 Register (CR39)

Read/Write Address: 3?5H, Index 39H
Power-On Default: 00H

Loading 101xxxxx (e.g., A0H) unlocks the extended CRTC registers from CR40 through CRFF for reading/writing (x = don't care). Loading A5H allows bits 7-2 of CR36, bits 7-0 of CR37, bits 7-0 of CR68 and bits 7-0 of CR6F to be written and also selects the CTR registers at Indexes 22H-29H instead of the CR registers at those same indices.

7	6	5	4	3	2	1	0
= 1	= 0	= 1					

Miscellaneous 1 Register (CR3A)

Read/Write Address: 3?5H, Index 3AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
PCIRB DISA	R	HST DFW	ENH 256	TOP MEM	R	R	R

Bits 2–0 Reserved

Bit 3 TOP MEM - Enable Top of Memory Access
0 = Top of memory access disabled
1 = Simultaneous VGA text and Enhanced modes are enabled. CPU and CRTC accesses are then directed to the top 32- or 64-KByte area of display memory depending on whether address bit 13 is 0 or 1 respectively.

Bit 4 ENH 256 - Enable 8 Bits/Pixel or Greater Color Enhanced Mode
0 = Attribute controller shift registers configured for 4-bit modes
1 = Attribute controller shift register configured for 8-, 16- and 24/32-bit color Enhanced modes

Bit 5 HST DFW - Enable High Speed Text Font Writing
0 = Disable high speed text font writing
1 = Enable high speed text font writing

Setting this bit to 1 is only required for DCLK rates greater than 40 MHz. See bit 6 of CR31.

Bit 6 Reserved

Bit 7 PCIRB DISA - PCI Read Bursts Disabled
0 = PCI read burst cycles enabled
1 = PCI read burst cycles disabled

Note: Bit 7 of CR66 must be set to 1 before this bit is set to 1.

Start Display FIFO Register (CR3B)

Read/Write Address: 3?5H, Index 3BH
Power-On Default: 00H Paired

This value must lie in the horizontal blanking period and is typically 5 less than the value programmed in CR0. This parameter helps to ensure that adequate time is available during horizontal blanking for activities such as RAM refresh that require control of the display memory. Bit 9 of this value is bit 6 of CR5D. This register must be enabled by setting bit 4 of CR34 to 1 and CR63_4-3 to 01b.

7	6	5	4	3	2	1	0
START DISPLAY FIFO FETCH							

Bits 7–0 START DISPLAY FIFO FETCH
9-bit Value = the time in character clocks from the active display start until the restart of fetching of FIFO data after the start of horizontal blanking. This register contains the low-order 8 bits of this value.

Interlace Retrace Start Register (CR3C)

Read/Write Address: 3?5H, Index 3CH
Power-On Default: 00H Paired

This value allows determination of the even/odd row active display starting positions when operating in an interlaced mode. This register is enabled by bit 5 of CR42.

7	6	5	4	3	2	1	0
INTERLACE RETRACE START POSITION							

Bits 7–0 INTERLACE RETRACE START POSITION
Value = offset in terms of character clocks for Interlaced mode start/end in even/odd frames.

NTSC/PAL Control Register (CR3D)

Read/Write Address: 3?5H, Index 3DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
NT	R	N/P	B/W	R	TV OUTPUT		TV

Bit 0 TV - Enable TV Mode
0 = Disable TV mode
1 = Enable TV mode

Bit 2-1 TV OUTPUT
00 = AY = luma; AC = chroma (S-Video)
01 = Reserved
10 = Reserved
11 = AY = composite; AC = composite (NTSC/PAL)

Bit 3 Reserved

Bit 4 B/W - Black and White Video
0 = Color TV output
1 = Black and white TV output

Bit 5 N/P = NTSC/PAL
0 = NTSC output
1 = PAL output

Bit 6 Reserved

Bit 7 NT - NTSC Type
0 = U.S. NTSC
1 = Japanese NTSC

Vertical Counter Register (CR3E)

Read/Write Address: 3?5H, Index 3EH
Power-On Default: 00H

7	6	5	4	3	2	1	0
VERTICAL COUNTER BITS 10-3							

Bits 7–0 VERTICAL COUNTER BITS 10-3

A read of this register is valid only if two consecutive reads return the same value.

System Configuration Register (CR40)

Read/Write Address: 3?5H, Index 40H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R = 0

Bit 0 Reserved = 0

Bits 7–1 Reserved

BIOS Flag Register (CR41)

Read/Write Address: 3?5H, Index 41H
Power-On Default: 00H

7	6	5	4	3	2	1	0
BIOS-FLAG-REGISTER-1							

Bits 7–0 BIOS-FLAG-REGISTER-1
Used by the video BIOS.

Mode Control Register (CR42)

Read/Write Address: 3?5H, Index 42H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	INTL MODE	R	R	R	R	R

Bits 4–0 Reserved

Bit 5 INTL MODE - Interlaced Mode
0 = Noninterlaced
1 = Interlaced

This bit enables the function of CR3C.

Note: This bit is paired.

Bits 7–6 Reserved

Extended Mode Register (CR43)

Read/Write Address: 3?5H, Index 43H
Power-On Default: 00H Paired

7	6	5	4	3	2	1	0
HCTR X2	CURSOR BLINK		R	CHR BLNK	R	R	R

Bits 2–0 Reserved

Bit 3 CHR BLNK - Character Blink Control
0 = Blink every 32 frames
1 = Blink every 64 frames

Bit 4 Reserved

Bits 6–5 CURSOR BLINK
00 = Blink every 16 frames
01 = Blink every 32 frames
1x = Blink every 64 frames

Bit 7 HCTR X2 - Horizontal Counter Double Mode
0 = Disable horizontal counter double mode
1 = Enable horizontal counter double mode (horizontal CRT parameters are doubled)

Hardware Graphics Cursor Mode Register (CR45)

Read/Write Address: 3?5H, Index 45H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	HWGC 1280	R	R	HCP	HWGC ENB

Bit 0 HWGC ENB - Hardware Graphics Cursor Enable
0 = Hardware graphics cursor disabled in any mode
1 = Hardware graphics cursor enabled in Enhanced mode

Bit 1 HCP - Hardware Cursor Position
0 = Hardware cursor position can be changed more than once in a frame. The last written cursor position will take effect in the next frame.
1 = Hardware cursor position cannot be changed more than once a frame

Bits 3-2 Reserved

Bit 4 HWGC 1280 - Hardware Cursor Right Storage
0 = Function disabled
1 = For 8 bits/pixel, the last 512 bytes in each 2-KByte line of the hardware cursor start address become the hardware graphics cursor storage area. Bits 1-0 of CR4D must be 11b.

Bits 7–5 Reserved

Hardware Graphics Cursor Origin-X Registers (CR46, CR47)

Read/Write Address: 3?5H, Index 46H, 47H
Power-On Default: 0000H

The high order three bits are written into CR46 and the low order byte is written into CR47.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG X (H)			HWGC ORG X (L)							

Bits 10–0 HWGC ORG X(H) (L) - X-Coordinate of Cursor Left Side

Bits 15–11 Reserved

Hardware Graphics Cursor Origin-Y Registers (CR48, CR49)

Read/Write Address: 3?5H, Index 48H, 49H
Power-On Default: Undefined

The high order three bits are written into CR48 and the low order byte is written into CR49.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG Y (H)			HWGC ORG Y (L)							

Bits 10–0 HWGC ORG Y (H)(L) - Y-Coordinate of Cursor Upper Line
The cursor X, Y position is registered upon writing HWGC ORG Y (H).

Bits 15–11 Reserved

Hardware Graphics Cursor Foreground Color Stack Register (CR4A)

Read/Write Address: 3?5H, Index 4AH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR FOREGROUND STACK (0-2)							

Bits 7–0 TRUE COLOR FOREGROUND STACK (0-2)

Three foreground color registers are stacked at this address. The stack pointer (common with CR4B) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4A) increments the stack pointer by 1, so three writes provide 24 bits of true color information.

Hardware Graphics Cursor Background Color Stack Register (CR4B)

Read/Write Address: 3?5H, Index 4BH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR BACKGROUND STACK (0-2)							

Bits 7–0 TRUE COLOR BACKGROUND STACK (0-2)

Three background color registers are stacked at this address. The stack pointer (common with CR4A) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4B) increments the stack pointer by 1, so three writes provide 24 bits of true color information.

Hardware Graphics Cursor Storage Start Address Registers (CR4C, CR4D)

Read/Write Address: 3?5H, Index 4CH, 4DH
Power-On Default: Undefined

The high order four bits are written into CR4C and the low order byte is written into CR4D.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	HWGC STA(H)				HWGC STA(L)							

Bits 11–0 HWGC STA(H)(L) - Hardware Graphics Cursor Storage Start Address

Bits 15–12 Reserved

Hardware Graphics Cursor Pattern Display Start X-PXL-Position Register (CR4E)

Read/Write Address: 3?5H, Index 4EH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START X-POS					

Bits 5–0 HWGC PAT DISP START X-POS - HWGC Pattern Display Start-X Pixel Position

This value is the offset (in pixels) from the left side of the 64x64 cursor pixel pattern from which the cursor is displayed. This allows a partial cursor to be displayed at the left border of the display.

Bits 7–6 Reserved

Hardware Graphics Cursor Pattern Disp Start Y-PXL-Position Register (CR4F)

Read/Write Address: 3?5H, Index 4FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START Y-POS					

Bits 5–0 HWGC PAT DISP START Y-POS - HWGC Pattern Display Start-Y Pixel Position

This value is the offset (in pixels) from the top of the 64x64 cursor pixel pattern from which the cursor is displayed. This allows a partial cursor to be displayed at the top of the display.

Bits 7–6 Reserved

Software Register (CR50)

Read/Write Address: 3?5H, Index 50H
Power-On Default: 00H

7	6	5	4	3	2	1	0
RESERVED FOR S3 SOFTWARE							

Bits 7–0 RESERVED FOR S3 SOFTWARE

Extended System Control 2 Register (CR51)

Read/Write Address: 3?5H, Index 51H
Power-On Default: 00H Paired

7	6	5	4	3	2	1	0
SPRL	R	LOG-SCR-W 9	8	R	R	R	R

Bits 3–0 Reserved

Bits 5–4 LOG-SCR-W - Logical Screen Width Bits 9-8
These are two extension bits of the Offset register (CR13)

Note: These bits are paired.

Bit 6 Reserved

Bit 7 SPRL - Streams Processor Register Load Enable
0 = No effect
1 = Enable loading of the shadowed Streams Processor registers

This bit is effective only when CR66_5 =1 and is automatically cleared to 0 after it is set.

Extended BIOS Flag 1 Register (CR52)

Read/Write Address: 3?5H, Index 52H
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-1							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-1

See the S3 video BIOS documentation for the coding of this register.

Extended Memory Control 1 Register (CR53)

Read/Write Address: 3?5H, Index 53H
Power-On Default: See Bit Descriptions

7	6	5	4	3	2	1	0
R	SWP NBL	MMIO WIN	MMIO SELECT		BIG ENDIAN LIN ADDR		R

Bit 0 Reserved

Bits 2-1 BIG ENDIAN LIN ADDR - Big Endian Data Byte swap (linear addressing only)
00 = No swap (Default)
01 = Swap bytes within each word
10 = Swap all bytes in doublewords (bytes reversed)
11 = Reserved

Bits 4-3 MMIO SELECT
00 = Disable MMIO
01 = New MMIO (relocatable) enabled (Default for PCI)
10 = Trio64-type MMIO enabled at window selected by bit 5 of this register
11 = Trio64-type MMIO and new MMIO enabled

Refer to the MMIO explanation in Section 15 for more information.

Bit 5 MMIO WIN - Trio64-type MMIO Window
0 = Trio64-type MMIO window enabled at A8000H - AFFFFH. A0000H - A7FFF available for image transfers (Default)
1 = Trio64-type MMIO window enabled at B8000H - BFFFFH. A0000H - B7FFFH are not used (no image transfer area)

Bits 4-3 of this register must be programmed to 10b for this bit to be effective.

Bit 6 SWP NBL - Swap Nibbles
0 = No nibble swap (Default)
1 = Swap nibbles in each byte of a linear memory address read or write operation

Bit 7 Reserved

Extended Memory Control 2 Register (CR54)

Read/Write Address: 3?5H, Index 54H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	M	BIG ENDIAN	

Bits 1–0 BIG ENDIAN - Big Endian Data Byte Swap (not linear addressing or image writes)
00 = No swap (Default)
01 = Swap bytes within each word
10 = Swap all bytes in doublewords (bytes reversed)
11 = Swap according to C/BE[3:0]

Byte enable settings for a bit setting of 11b:
0000 = Swap all bytes in doublewords (bytes reversed)
0011 = Swap bytes within selected word
1100 = Swap bytes within selected word
All other values = no swap

Bits 7–2 Reserved

Hardware Cursor/Icon Select Register (CR55)

Read/Write Address: 3?5H, Index 55H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	HC/I	R	R	R	R	R

Bits 4–0 Reserved

Bit 5 HC/I - Hardware Cursor/Icon Display Enable
0 = Enable hardware icon display
1 = Enable hardware cursor display

This bit is only effective when SR33_5 = 1.

Bits 7–6 Reserved

External Sync Control 1 Register (CR56)

Read/Write Address: 3?5H, Index 56H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	DIS VSYN	DIS HSYN	R

Bit 0 Reserved

Bit 1 DIS HSYN - Tri-state off HSYNC
0 = HSYNC output buffer tri-stated on
1 = HSYNC output buffer tri-stated off

Bit 2 DIS VSYN - Tri-state off VSYNC
0 = VSYNC output buffer tri-stated on
1 = VSYNC output buffer tri-stated off

Bits 7–3 Reserved

Linear Address Window Control Register (CR58)

Read/Write Address: 3?5H, Index 58H
Power-On Default: 10H

7	6	5	4	3	2	1	0
R	R	R	ENB LA	R	R	LAW-SIZE 1	0

Bits 1–0 LAW-SIZE - Linear Address Window Size
00 = 64 KBytes (Default)
01 = Reserved
10 = 2 MBytes
11 = 4 MBytes

The 64K window is not available if new MMIO is enabled (CR53_3 = 1).

Bits 3-2 Reserved

Bit 4 ENB LA - Enable Linear Addressing for Enhanced Modes
0 = Disable linear addressing
1 = Enable linear addressing (Default)

Enabling linear addressing disables access to the A000H-AFFFH region unless the window size is set to 64K via bits 1-0 of this register and A000H is specified as the base in CR59-5A. CR66_6 enables linear addressing for non-enhanced modes

Bits 7–5 Reserved

Linear Address Window Position Registers (CR59-5A)

Read/Write Address: 3?5H, Index 59H-5AH
Power-On Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINEAR-ADDRESS-WINDOW-POSITION															

CR59 contains the upper byte (15-8) and CR5A contains the lower byte (7-0). These registers specify the Linear Address Window Position in 32-bit CPU address space. The Linear Address Window resides on a 64KB, 1MB. 2MB or 4MB memory boundary (size-aligned boundary). Some LSBs of this register (illustrated by "xx..xx" in the following table) are ignored because of the size-aligned boundary scheme.

LAW Size	Linear Address Window Position Register Bit(s)									
64KB	31-25	24	23	22	21	20	19	18	17	16
2MB	31-25	24	23	22	21	xx	xx	xx	xx	xx
4MB	31-25	24	23	22	xx	xx	xx	xx	xx	xx

Bits 15–0 LINEAR-ADDRESS-WINDOW-POSITION - LA Window Position Bits 31-16
16-bit Value = the linear address window position in 32-bit CPU address space.

Bits 15-0 are common with bits 31-16 of the base address programmed into the PCI Base Address 0 register at address 10H-12H. Writes to these bits in either register will also be written to the other. Writes to CR59 and CR5A should be read-modify- writes that do not change the upper 6 bits, as these bits are written by the system BIOS to place ViRGE/MX in a unique address space. Note that system BIOS writes will leave bits 9-0 in an indeterminate state, so these should be properly initialized before linear addressing is enabled.

If a 64K window is specified, bits 5-0 of CR6A specify the 64K page of display memory to be accessed through a 64K window located at the address specified in these registers.

If new MMIO is enabled (CR53_3 = 1), the base address is specified by CR59_7-2 (or bits 31-26 of the PCI Base Address 0 register). This is concatenated with the display memory address specified by the programmer.

General Output Port Register (CR5C)

Read/Write Address: 3?5H, Index 5CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
GENERAL-OUT-PORT							

Bits 7–0 GENERAL-OUT-PORT

This register can be used in a variety of ways. See Section 13 for a complete description.

Extended Horizontal Overflow Register (CR5D)

Read/Write Address: 3?5H, Index 5DH
Power-On Default: 00H Paired

7	6	5	4	3	2	1	0
R	SFF 8	HSP	SHS 8	HBP	SHB 8	HDE 8	HT 8

Bit 0 HT 8 - Horizontal Total (CR0) Bit 8

Bit 1 HDE 8 - Horizontal Display End (CR1) Bit 8

Bit 2 SHB 8 - Start Horizontal Blank (CR2) Bit 8

Bit 3 HBP - Horizontal Blank Period
0 = Horizontal blank period is equal to or less than 64 character clocks
1 = Horizontal blank period is greater than 64 character clocks

See CR3_4-0.

Bit 4 SHS 8 - Start Horizontal Sync Position (CR4) Bit 8

Bit 5 HSP - Horizontal Sync Period
0 = Horizontal sync period is equal to or less than 32 character clocks
1 = Horizontal sync period is greater than 32 character clocks

See CR5_4-0.

Bit 6 SFF 8 - Start FIFO Fetch (CR3B) Bit 8

Bit 7 Reserved

Extended Vertical Overflow Register (CR5E)

Read/Write
Power-On Default: 00H
Address: 3?5H, Index 5EH
Paired

7	6	5	4	3	2	1	0
R	LCM 10	R	VRS 10	R	SVB 10	VDE 10	VT 10

Bit 0 VT 10 - Vertical Total (CR6) Bit 10

Bit 1 VDE 10 - Vertical Display End (CR12) Bit 10

Bit 2 SVB 10 - Start Vertical Blank (CR15) Bit 10

Bit 3 Reserved

Bit 4 VRS 10 - Vertical Retrace Start (CR10) Bit 10

Bit 5 Reserved

Bit 6 LCM 10 - Line Compare Position (CR18) Bit 10

Bit 7 Reserved

Extended Memory Control 3 Register (CR60)

Read/Write
Power-On Default: 00H
Address: 3?5H, Index 60H

7	6	5	4	3	2	1	0
R	R	R	R	SDRAM/SGRAM CLOCK CTL			

Bits 3-0 SDRAM/SGRAM CLOCK CTL
0000 = No effect on SDCLK
0001 = SDCLK generated approximately 9 ns earlier than for the 0000 setting
0010 = SDCLK generated approximately 8 ns earlier than for the 0000 setting
.
.
1001 = SDCLK generated approximately 1 ns earlier than for the 0000 setting
1010 = SDCLK generated approximately 1 ns later than for the 0000 setting
.
.
1111 = SDCLK generated approximately 6 ns later than for the 0000 setting

Bits 7-4 Reserved

Extended Memory Control 4 Register (CR61)

Read/Write Address: 3?5H, Index 61H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	BIG ENDIAN		R	R	R	R	R

Bits 4-0 Reserved

Bits 6-5 BIG ENDIAN - Big Endian Data Bye Swap (image writes only)
00 = No swap (Default)
01 = Swap bytes within each word
10 = Swap all bytes in doublewords (bytes reversed)
11 = Reserved

Bit 7 Reserved

Start FIFO Fetch Register (CR63)

Read/Write Address: 3?5H, Index 63H
Power-On Default: 00H Paired

7	6	5	4	3	2	1	0
R	R	R	FIFO FETCH		R	R	HT

Bit 0 HT - HSYNC Timing
0 = HSYNC timing is compatible with VGA standard for CRT VGA modes
1 = HSYNC timing is determined by programming of horizontal retrace start and end registers for CRT VGA modes

Bits 2-1 Reserved

Bits 4-3 FIFO FETCH - Start Display FIFO Fetch
00 = Start FIFO fetch on falling edge of the internal HSYNC signal
01 = Start FIFO fetch at value programmed in CR3B
10 = Start FIFO fetch on rising edge of the internal HSYNC signal delayed by 4 character clocks
11 = Start FIFO fetch on rising edge of the internal HSYNC signal delayed by 6 character clocks

Bits 7-5 Reserved

Extended Miscellaneous Control Register (CR65)

Read/Write Address: 3?5H, Index 65H
Power-On Default: 00H Paired

7	6	5	4	3	2	1	0
			DLY BLANK				
R	R	R	1	0	R	R	R

Bits 2-0 Reserved

Bits 4-3 DLK BLANK - Delay $\overline{\text{BLANK}}$ by DCLK
00 = No delay of $\overline{\text{BLANK}}$
01 = Delay $\overline{\text{BLANK}}$ for 1 DCLK
10 = Delay $\overline{\text{BLANK}}$ for 2 DCLKs
11 = Delay $\overline{\text{BLANK}}$ for 3 DCLKs

Note: These bits are paired.

Bits 7-5 Reserved

Extended Miscellaneous Control 1 Register (CR66)

Read/Write Address: 3?5H, Index 66H
Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI DE	ELA	SPRL	R	PCI DIS	R	SW RST	EN ENH

Bit 0 EN ENH - Enable Enhanced Functions
0 = Disable enhanced functions
1 = Enable enhanced functions

This bit must be programmed during screen off (SR1_5 or CR71_5 = 1) or during the vertical retrace period. Setting SR1_5 to 1 may take up to 3 HSYNCs to take effect.

Note: This bit is paired.

Bit 1 SW RST - Software Reset
0 = No function
1 = Software reset of the S3d Engine

Bit 2 Reserved

Bit 3 PCI DIS - PCI Disconnect
0 = No effect
1 = An attempt to write data with the Command FIFO or LPB output FIFO full or to read data with the Command FIFO not empty generates a PCI bus disconnect cycle

Bit 7 of this register must also be set to 1 to enable this feature.

Bit 4 Reserved

Bit 5 SPRL - Streams Processor Register Load Control
0 = Load active registers on VSYNC active
1 = Load active registers immediately when programmed

New values programmed to certain Streams Processor registers (identified in the register descriptions) normally take effect on the next VSYNC. This delay is overridden by setting this bit.

Bit 6 ELA - Enable Linear Addressing in Non-Enhanced Modes
0 = Standard VGA address translation is used for CPU accesses to video memory
1 = Linear addressing used for CPU video memory accesses

For non-enhanced modes, CR66_0 = 0 and MM850C_0 = 0. This option can be used to write icon or cursor data.

Bit 7 PCI DE - PCI bus disconnect enable
0 = PCI bus disconnect disabled
1 = PCI bus disconnect enabled

Setting this bit to 1 allows PCI burst cycles to be interrupted if AD[1:0] ≠ 00b or if the address during the burst goes outside the address ranges supported by ViRGE/MX. See also bit 3 of this register.

Extended Miscellaneous Control 2 Register (CR67)

Read/Write Address: 3?5H, Index 67H
Power-On Default: 00H

7	6	5	4	3	2	1	0
COLOR MODE				R	SM	R	R

Bits 1-0 Reserved

Bit 2 SM - Streams Mode
0 = Streams Processor disabled
1 = Streams Processor enabled

The Streams Processor must only be enabled during the vertical retrace period.

Bit 3 Reserved

Bits 7–4 COLOR MODE - DAC Color Mode
0000 = 4- or 8-bit color, 1 pixel/VCLK
0011 = 15-bit color, 1 pixel/VCLK
0101 = 16-bit color, 1 pixel/VCLK
0111 = 24-bit color (packed), 1 pixel/VCLK
1101 = 24-bit color, (not packed) 1 pixel/VCLK

All other mode values are reserved.

Note: These bits are paired.

Configuration 3 Register (CR68)

Read/Write Address: 3?5H, Index 68H
Power-On Default: Depends on Strapping

This is of the power-on strapping bits (along with CR36, CR37 and CR6F). PD[23:16] are sampled on power-on reset and their states are written to bits 7-0 of this register. These pins have internal pull-downs and the states of pins are inverted during reset, so the bits with pull-downs will default to 1's if no pins are pulled up. A5H must be written to CR39 to provide read/write access to this register.

7	6	5	4	3	2	1	0
MTS		RAS - PCG		RL	SES	CAS/OE STR	

Bits 1-0 $\overline{\text{CAS}}$ Stretch Time (EDO DRAM)
00 = approximately 1.5 ns stretch (nominal)
01 = approximately 1.0 ns stretch (nominal)
10 = approximately 0.5 ns stretch (nominal)
11 = no stretch

This parameter adjusts the timing for the edges of the $\overline{\text{CAS}}$ signals selected by bit 2. This allows stretching of the signal active time for $\overline{\text{CAS}}$ to allow more time for valid pixel data to be available. The delay time shown above is an approximation. It is affected by both process and signal loading and must be measured for each design.

SDRAM/SGRAM Auto Refresh to New Command
00 = 7 MCLKs
01 = 8 MCLKs
10 = 9 MCLKs
11 = 10 MCLKs

This is the time from a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle to the next refresh cycle or activation command.

Bit 2 SES - Stretch Edge Select
0 = Stretch $\overline{CAS}$, $\overline{WE}$ and $\overline{OE}$ rising edges by the amounts determined by CR68_1-0, CR6F_4-3 and CR6F_6-5 respectively
1 = Stretch $\overline{CAS}$, $\overline{WE}$ and $\overline{OE}$ falling edges by the amounts determined by CR68_1-0, CR6F_4-3 and CR6F_6-5 respectively

SDRAM/SGRAM Last Data In to Row Precharge Delay (Write Cycle)
0 = 1 MCLK
1 = 2 MCLKs

Bit 3 RL - Minimum $\overline{RAS}$ Low Timing Select (EDO DRAM)
0 = 3.5 MCLKs
1 = 2.5 MCLKs

This parameter specifies the length of the $\overline{RAS}$ active time for a single row/column access. $\overline{RAS}$ may be held low longer to accommodate additional page mode accesses to the same row.

Minimum $\overline{SDRAS}$ Low to Following Precharge Timing Select
0 = 6 MCLKs
1 = 7 MCLKs

This value assumes a single command (e.g., read) is executed. The time will extend one clock for each additional command.

Bits 5-4 $\overline{RAS}$-PCG - $\overline{RAS}$ Precharge Timing Select (EDO DRAM)
00 = Reserved
01 = 3.5 MCLKs
10 = 2.5 MCLKs
11 = 1.5 MCLKs

When $\overline{RAS}$ goes high to end a memory cycle, this parameter specifies the minimum period it must be held high before beginning another memory access cycle.

$\overline{SDRAS}$ Precharge Time
00 = Reserved
01 = Reserved
10 = 4 MCLKs
11 = 3 MCLKs

This is the time from a precharge cycle to a refresh cycle (if required) or to the next activation command.

Bits 7-6 MTS - Memory Type Select
00 = 256Kx8
01 = 256Kx32
10 = 512Kx32
11 = 256Kx16

This field applies to both DRAM and synchronous RAM.

Extended System Control 3 Register (CR69)

Read/Write Address: 3?5H, Index 69H
Power-On Default: 00H Paired

7	6	5	4	3	2	1	0
R	R	R	R	DISP-START-ADDR			

Bits 3–0 DISP-START-ADDR
This field contains the upper 4 bits (19-16) of the display start address, allowing addressing of up to 4 MBytes of display memory.

Bits 7–4 Reserved

Extended System Control 4 Register (CR6A)

Read/Write Address: 3?5H, Index 6AH
Power-On Default: 00H Paired

7	6	5	4	3	2	1	0
R	R	CPU-BASE-ADDRESS					

Bits 5–0 CPU-BASE-ADDRESS
This field contains the upper 6 bits (19-14) of the CPU base address, allowing accessing of up to 4 MBytes of display memory via 64K pages. If linear addressing is enabled and a 64 KByte window is specified, these bits specify the 64K page to be accessed at the base address specified in CR59 and CR5A. Otherwise, the base address is normally at A000H.

Bits 7–6 Reserved

Extended BIOS Flag 3 Register (CR6B)

Read/Write Address: 3?5H, Index 6BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-3							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-3
This register is reserved for use by the S3 BIOS.

Extended BIOS Flag 4 Register (CR6C)

Read/Write Address: 3?5H, Index 6CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-4							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-4
This register is reserved for use by the S3 BIOS.

Extended BIOS Flag 5 Register (CR6D)

Read/Write Address: 3?5H, Index 6DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-5							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-5
This register is reserved for use by the S3 BIOS.

DAC Signature Test Data Register (CR6E)

Read/Write Address: 3?5H, Index 6EH
Power-On Default: 00H

7	6	5	4	3	2	1	0
DAC SIGNATURE TEST DATA							

Bits 7–0 DAC SIGNATURE TEST DATA

See Section 10.5 for a description of signature testing.

Configuration 4 Register (CR6F)

Read/Write Address: 3?5H, Index 6FH
Power-On Default: Depends on Strapping

This is the fourth byte of power-on strapping bits. PD[31:24] are sampled at reset and the values are written to bits 7-0 of this register. A5H must be written to CR39 to provide read/write access to this register. Non-reserved bits will power up with a value of 1 if the corresponding pins are not pulled high.

7	6	5	4	3	2	1	0
SCS	OE DELAY		WE DELAY		IOEN	IOSEL	F/R

Bit 0 F/R - FPPOL/$\overline{\text{ROMEN}}$ Select
0 = Select ROMEN function for the FPPOL/ROMEN pin
1 = Select FPPOL function for the FPPOL/ROMEN pin

Bit 1 IOSEL - Serial Port I/O Address Select
0 = MMFF20 is accessed at I/O address 000E8H
1 = MMFF20 is accessed at I/O address 000E2H

Bit 2 of this register must be cleared to 0 for this bit to have effect.

Bit 2 IOEN - Serial Port Address Type Select
0 = MMFF20 is accessed either at the I/O port defined in bit 1 of this register or at its MMIO address
1 = MMFF20 is accessed at its MMIO address only (no I/O)

Enabling I/O access allows the serial port to be used for I^2C communications when ViRGE/MX is disabled.

Bits 4-3 WE Delay (EDO DRAM)
00 = 1.5 ns delay
01 = 1.0 ns delay
10 = 0.5 ns delay
11 = no delay

The edge being delayed is specified by CR68_2.

SDRAM/SGRAM Time Interval Select for Consecutive Bank Activation (Bit 3)
0 = 2 MCLKs
1 = 3 MCLK

SDRAM/SGRAM Last Data Out to Row Precharge Delay (Bit 4) (Read Cycle)
0 = -2 MCLKs
1 = -1 MCLK

Bits 6-5 OE DELAY (EDO DRAM)
00 = 1.5 ns (nominal)
01 = 1.0 ns (nominal)
10 = 0.5 ns (nominal)
11 = No delay

The edge being delayed is specified by CR68_2.

SDRAM/SGRAM $\overline{CAS}$ Latency
00 = 4 MCLKs
01 = 4 MCLKs
10 = 2 MCLKs
11 = 3 MCLKs

Bit 7 SDRAM/SGRAM Clock Select
0 = Internal clock is used to latch SDRAM/SGRAM read data
1 = SDCLKI input used to latch SDRAM/SGRAM read data

This bit is normally set to 1 for clock speeds greater than 66 MHz.

Dual Image Control Register (CR71)

Read/Write Address: 3?5H, Index 71H
Power-On Default: 00H Paired

7	6	5	4	3	2	1	0
R	R	SOFF	R	R	R	SOC	R

Bit 0 Reserved

Bit 1 SOC - Screen Off Control
0 = Use SR1_5 for screen off control
1 = Use CR71_5 for screen off control

Bits 4-2 Reserved

Bit 5 SOFF - Screen Off
0 = Screen on
1 = Screen off

This is the same as blanking. The control signals are still active. When this bit is set, up to 3 HSYNCs may elapse before the screen is turned off. Software must be careful to allow this amount of time to pass before writing to registers that must be programmed during screen off.

Bits 7-6 Reserved

Extended Memory Control 5 Register (CR72)

Read/Write Address: 3?5H, Index 72H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	SMS	R	R	R	R	R

Bits 4-0 Reserved

Bit 5 SMS - SDRAM/SGRAM Mode Set
0 = No effect
1 = SDRAM/SGRAM mode set and power up initialization generated

After the $\overline{CAS}$ latency is programmed (typically via power-on strapping), this bit is programmed to 1 to generate an SDRAM/SGRAM mode programming cycle. This bit is automatically cleared to 0 after the programming cycle.

Bits 7-6 Reserved

Extended Memory Control 7 Register (CR74)

Read/Write Address: 3?5H, Index 74H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	BRAS	BRBS	MRT			DRD

Bit 0 DRD - Distributed Refresh Disable
0 = Distributed refresh enabled
1 = Memory is refreshed after the end of every line (blanking)

This applies to standard EDO DRAM refresh or auto refresh for SDRAM/SGRAM. The frequency of refreshes is specified via SR75_7-0.

Bits 3-1 MRT - Memory Refresh Type During Power Down
000 = EDO or SDRAM/SGRAM self refresh
001 = SDRAM/SGRAM power-down
010 = Reserved
011 = Reserved
100 = EDO DRAM normal 8 ms refresh
101 = EDO DRAM 16 ms slow refresh
110 = EDO DRAM 64 ms slow refresh
111 = EDO DRAM 128 ms slow refresh

Bit 4 BRBS - Burst Refresh Before Self Refresh for EDO and SDRAM
0 = Burst refresh will be done before going into self refresh
1 = Burst refresh will not be done before going into self refresh

Bit 5 BRAS - Burst Refresh After Self Refresh for EDO and SDRAM
0 = Burst refresh will be done after coming out of self refresh
1 = Burst refresh will not be done after coming out of self refresh

Bit 7-6 Reserved

Extended Memory Control 8 Register (CR75)

Read/Write Address: 3?5H, Index 75H
Power-On Default: 00H

7	6	5	4	3	2	1	0
REFRESH COUNT FOR DISTRIBUTED REFRESH							

Bits 7-0 REFRESH COUNT FOR DISTRIBUTED REFRESH

For CR74_0 = 0 (distributed refresh)

decimal value = (RTxMCLKx1000/RC) - 273, where:

RT = refresh time in ms
RC = refresh cycles per refresh time
MCLK = memory clock speed in MHz

Convert the decimal value generated by the above equation to binary and eliminate the 3 lsb's. The remaining digits become the lsb's of the value to be programmed into this register. Padding of msb's with 0's may be required to form an 8-digit value. These 8 bits are the msb's of the 11-bit internal refresh counter. The 3 lsb's of the counter are forced to 111b.

For CR74_0 = 1 (refresh during blanking)

value = number of refreshes to be performed during each blanking period. Only bits 3-0 are used.

Memory Cycle Control 1 Register (CR76)

Read/Write Address: 3?5H, Index 76H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	1MC

Bit 0 1MC - 1-cycle CPU Accesses
0 = Use 2 MCLK CPU linear addressing accesses to video memory
1 = Use 1 MCLK CPU linear addressing accesses to video memory

This bit is valid for all modes. In practice, however, it should only be set to 1 in Enhanced mode. SR15_7 and this this bit must always be set to the same value.

Bits 7-1 Reserved

Memory Cycle Control 2 Register (CR77)

Read/Write Address: 3?5H, Index 77H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	MABS	MDBS	SBS	

Bit 0 Reserved

Bit 1 SBS - SDCLK Buffer Strength
0 = 8 mA
1 = 16 mA

Bit 2 MDBS - Memory Data (PD[63:0]) Buffer Strength
0 = 4 mA
1 = 8 mA

Bit 3 MABS - Memory Address (MA[10:0]) Buffer Strength
0 = 4 mA
1 = 8 mA

Bits 7-4 Reserved

Memory Timing Control Register (CR78)

Read/Write Address: 3?5H, Index 78H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	RRD

Bit 0 RRD - $\overline{\text{RAS}}$ Rising Edge Delay
0 = No effect
1 = $\overline{\text{RAS}}$ rising edge delayed by 0.5 MCLK

Setting this bit reduces the $\overline{\text{RAS}}$ precharge (set via CR68_5-4) and increases the $\overline{\text{RAS}}$ low time. This may be required for fast EDO DRAM.

Bits 7-1 Reserved

Primary Stream 1 Timeout Register (CR7B)

Read/Write Address: 3?5H, Index 7BH
Power-On Default: 0BH

7	6	5	4	3	2	1	0
PS1 TIMEOUT							

Bits 7-0 PS1 TIMEOUT

Value = # of MCLKs allocated to reading primary stream 1 data before memory bus control is withdrawn

Primary Stream 2 Timeout Register (CR7C)

Read/Write Address: 3?5H, Index 7CH
Power-On Default: 0BH

7	6	5	4	3	2	1	0
PS2 TIMEOUT							

Bits 7-0 PS2 TIMEOUT

Value = # of MCLKs allocated to reading primary stream 2 data before memory bus control is withdrawn

Secondary Stream Timeout Register (CR7D)

Read/Write Address: 3?5H, Index 7DH
Power-On Default: 0BH

7	6	5	4	3	2	1	0
SS TIMEOUT							

Bits 7-0 SS TIMEOUT

Value = # of MCLKs allocated to reading secondary stream data before memory bus control is withdrawn

STN Read Timeout Register (CR7F)

Read/Write Address: 3?5H, Index 7FH
Power-On Default: 0BH

7	6	5	4	3	2	1	0
STN READ TIMEOUT							

Bits 7-0 STN READ TIMEOUT

Value = # of MCLKs allocated to reading STN panel data before memory bus control is withdrawn

STN Write Timeout Register (CR80)

Read/Write Address: 3?5H, Index 80H
Power-On Default: 0BH

7	6	5	4	3	2	1	0
STN WRITE TIMEOUT							

Bits 7-0 STN WRITE TIMEOUT

Value = # of MCLKs allocated to writing STN panel data before memory bus control is withdrawn

LPB Write Timeout Register (CR81)

Read/Write Address: 3?5H, Index 82H
Power-On Default: 0BH

7	6	5	4	3	2	1	0
LPB WRITE TIMEOUT							

Bits 7-0 LPB WRITE TIMEOUT

Value = # of MCLKs allocated to LPB writes before memory bus control is withdrawn

Read DMA Timeout Register (CR82)

Read/Write Address: 3?5H, Index 82H
Power-On Default: 0BH

7	6	5	4	3	2	1	0
READ DMA TIMEOUT							

Bits 7-0 READ DMA TIMEOUT

Value = # of MCLKs allocated to DMA frame buffer reads before memory bus control is withdrawn

Host Interface Timeout Register (CR83)

Read/Write Address: 3?5H, Index 83H
Power-On Default: 0BH

7	6	5	4	3	2	1	0
HOST INTERFACE TIMEOUT							

Bits 7-0 HOST INTERFACE TIMEOUT

Value = # of MCLKs allocated to CPU accesses before memory bus control is withdrawn

S3d Engine Timeout Register (CR84)

Read/Write Address: 3?5H, Index 84H
Power-On Default: 0BH

7	6	5	4	3	2	1	0
S3d ENGINE TIMEOUT							

Bits 7-0 S3d ENGINE TIMEOUT

Value = # of MCLKs allocated to S3d Engine frame buffer accesses before memory bus control is withdrawn

Primary Stream 1 FIFO Threshold Register (CR85)

Read/Write Address: 3?5H, Index 85H
Power-On Default: 08H

7	6	5	4	3	2	1	0
R	R	R	PS1 FIFO THRESHOLD				

Bits 4-0 PS1 FIFO THRESHOLD

Value = # of FIFO slots

A memory bus control request is generated when the number of filled primary stream 1 FIFO slots is less than this value.

Bits 7-5 Reserved

Primary Stream 2 FIFO Threshold Register (CR86)

Read/Write Address: 3?5H, Index 86H
Power-On Default: 08H

7	6	5	4	3	2	1	0
R	R	R	PS2 FIFO THRESHOLD				

Bits 4-0 PS2 FIFO THRESHOLD

Value = # of FIFO slots

A memory bus control request is generated when the number of filled primary stream 2 FIFO slots is less than this value.

Bits 7-5 Reserved

Secondary Stream FIFO Threshold Register (CR87)

Read/Write Address: 3?5H, Index 87H
Power-On Default: 08H

7	6	5	4	3	2	1	0
R	R	R	SS FIFO THRESHOLD				

Bits 4-0 SS FIFO THRESHOLD

Value = # of FIFO slots

A memory bus control request is generated when the number of filled secondary stream FIFO slots is less than this value.

Bits 7-5 Reserved

STN Read FIFO Threshold Register (CR89)

Read/Write Address: 3?5H, Index 89H
Power-On Default: 08H

7	6	5	4	3	2	1	0
R	R	R	STN READ FIFO THRESHOLD				

Bits 4-0 STN READ FIFO THRESHOLD

Value = # of FIFO slots

A memory bus control request is generated when the number of filled STN read FIFO slots is less than this value.

Bits 7-5 Reserved

STN Write FIFO Threshold Register (CR8A)

Read/Write Address: 3?5H, Index 8AH
Power-On Default: 07H

7	6	5	4	3	2	1	0
R	R	R	R	STN WRITE THRESHOLD			

Bits 3-0 STN WRITE THRESHOLD

Value = # of FIFO slots

A memory bus control request is generated when the number of filled STN write FIFO slots is more than this value.

Bits 7-4 Reserved

LPB FIFO Threshold Register (CR8B)

Read/Write Address: 3?5H, Index 8BH
Power-On Default: 06H

7	6	5	4	3	2	1	0
R	R	R	LPB FIFO THRESHOLD				

Bits 4-0 LPB FIFO THRESHOLD

Value = # of FIFO slots

A memory bus control request is generated when the number of filled LPB FIFO slots is more than this value.

Bits 7-5 Reserved

Primary Stream FIFO Fetch Control 1 Register (CR90)

Read/Write Address: 3?5H, Index 90H
Power-On Default: 0xxxxxxxb Paired

7	6	5	4	3	2	1	0
EL1	R	R	R	R	L1 10-8		

Bits 2-0 L1 10-8 - Primary Stream L1 Parameter (Bits 10-8)
These are bits 10-8 of the primary stream L1 parameter. See the description of the primary stream L1 parameter in the description for CR91.

Bits 6-3 Reserved

Bit 7 EL1 - Enable L1 Parameter
0 = Primary stream display fetch length control (L1 parameter) disabled
1 = Primary stream display fetch length control (L1 parameter) enabled

Primary Stream FIFO Fetch Control 2 (CR91)

Read/Write Address: 3?5H, Index 91H
Power-On Default: Undefined Paired

These are the lower 8 bits of an 11-bit value used to optimize performance. The upper three bits are bits 2-0 of CR90.

7	6	5	4	3	2	1	0
L1 7-0							

Bits 7-0 L1 7-0 - Primary Stream L1 Parameter (Bits 7-0)
11-bit Value = [(number of bytes of displayed pixels per scan line) ÷ 8]. The number of bytes of displayed pixels per scan line must be even. A fractional result is rounded up to the nearest integer. This register contains the least significant 8 bits of this value.

Secondary Stream FIFO Fetch Control 1 Register (CR92)

Read/Write Address: 3?5H, Index 92H
Power-On Default: 0xxxxxxxb

7	6	5	4	3	2	1	0
EL2	R	R	R	R	L2 10-8		

Bits 2-0 L2 10-8 - Secondary Stream L2 Parameter (Bits 10-8)
These are bits 10-8 of the secondary stream L2 parameter. See the description of the primary stream L2 parameter in the description for CR93.

Bits 6-3 Reserved

Bit 7 EL2 - Enable L2 Parameter
0 = Secondary stream display fetch length control (L2 parameter) disabled
1 = Secondary stream display fetch length control (L2 parameter) enabled

Secondary Stream FIFO Fetch Control 2 (CR93)

Read/Write Address: 3?5H, Index 93H
Power-On Default: Undefined

These are the lower 8 bits of an 11-bit value used to optimize performance. The upper three bits are bits 2-0 of CR92.

7	6	5	4	3	2	1	0
L2 7-0							

Bits 7-0 L2 7-0 - Secondary Stream L2 Parameter (Bits 7-0)
11-bit Value = [(number of bytes of displayed pixels per scan line) ÷ 8] - 4. The number of bytes of displayed pixels per scan line must be even. This register contains the least significant 8 bits of this value.

PCI Subsystem Vendor ID Shadow Low Register (CR95)

Read/Write Address: 3?5H, Index 95H
Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI SUBSYSTEM VENDOR ID LOW BYTE							

Bits 7-0 PCI SUBSYSTEM VENDOR ID LOW BYTE

This register shadows the byte at PCI configuration space index 2CH.

PCI Subsystem Vendor ID Shadow High Register (CR96)

Read/Write Address: 3?5H, Index 96H
Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI SUBSYSTEM VENDOR ID HIGH BYTE							

Bits 7-0 PCI SUBSYSTEM VENDOR ID HIGH BYTE

This register shadows the byte at PCI configuration space index 2DH.

PCI Subsystem ID Shadow Low Register (CR97)

Read/Write Address: 3?5H, Index 97H
Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI SUBSYSTEM ID LOW BYTE							

Bits 7-0 PCI SUBSYSTEM ID LOW BYTE

This register shadows the byte at PCI configuration space index 2EH.

PCI Subsystem ID Shadow High Register (CR98)

Read/Write Address: 3?5H, Index 98H
Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI SUBSYSTEM ID HIGH BYTE							

Bits 7-0 PCI SUBSYSTEM ID HIGH BYTE

This register shadows the byte at PCI configuration space index 2FH.

Section 19: S3d Engine Register Descriptions

This section describes the S3d Registers. These registers are used to accelerate the display of 2D and 3D graphics.

In all register bit descriptions, the letter "R" identifies reserved bits (a reserved bit's read value is undefined unless noted, and you may write only zero to a reserved bit).

19.1 REGISTER MAPPING AND ADDRESSING

The S3d registers are memory-mapped starting at an offset of 100 A0000H from the base address. Table 19-1 shows the location of each register organized by drawing command type. All registers with the same mnemonic for different commands are the same register with multiple addresses. For example, at "xx" = D4, the three 2D commands use a register called SRC_BASE, with each of the 2D commands having a unique address for this register. Similarly, the two 3D commands share the Z-BASE register. The DEST_BASE register is shared by all commands at "xx" = D8. Each shared register is described only once in a section (2D or 3D) along with all of its addresses.

Table 19-1. S3d Register Memory Map

	Offset From Base Address (Little Endian Addressing)					
	100 A0xxH	100 A4xxH	100 A8xxH	100 ACxxH	100 B0xxH	100 B4xxH
xx	Pattern Registers	BitBLT/Rect Fill	2D Line	2D Polygon	3D Line	3D Triangle
D4		SRC_BASE	SRC_BASE	SRC_BASE	Z_BASE	Z_BASE
D8		DEST_BASE	DEST_BASE	DEST_BASE	DEST_BASE	DEST_BASE
DC		CLIP_L_R	CLIP_L_R	CLIP_L_R	CLIP_L_R	CLIP_L_R
E0		CLIP_T_B	CLIP_T_B	CLIP_T_B	CLIP_T_B	CLIP_T_B
E4		DEST_SRC_STR	DEST_SRC_STR	DEST_SRC_STR	DEST_SRC_STR	DEST_SRC_STR
E8		MONO_PAT_0		MONO_PAT_0	Z_STRIDE	Z_STRIDE
EC		MONO_PAT_1		MONO_PAT_1		TEX_BASE
F0		PAT_BG_CLR		PAT_BG_CLR		TEX_BDR_CLR
F4		PAT_FG_CLR	PAT_FG_CLR	PAT_FG_CLR	FOG_CLR	FOG_CLR
F8		SRC_BG_CLR				COLOR0
FC		SRC_FG_CLR				COLOR1
100	Start	CMD_SET	CMD_SET	CMD_SET	CMD_SET	CMD_SET
104	(100 to 1BC)	RWIDTH_HEIGHT				TBV
108		RSRC_XY				TBU
10C		RDEST_XY				TdWdX
110						TdWdY
114						TWS
118						TdDdX
11C						TdVdX
120						TdUdX
124						TdDdY
128						TdVdY
12C						TdUdY
130						TDS
134						TVS
138						TUS
13C						TdGdX_dBdX
140						TdAdX_dRdX
144					3dGdY_dBdY	TdGdY_dBdY
148					3dAdY_dRdY	TdAdY_dRdY
14C					3GS_BS	TGS_BS
150					3AS_RS	TAS_RS
154						TdZdX
158					3dZ	TdZdY
15C					3ZSTART	TZS
160						TdXdY12
164						TXEND12
168				PRdX		TdXdY01
16C			LXEND0_END1	PRXSTART	3XEND0_END1	TXEND01
170			LdX	PLdX	3dX	TdXdY02
174			LXSTART	PLXSTART	3XSTART	TXSTART02
178			LYSTART	PYSTART	3YSTART	TYSTART
17C			LYCNT	PYCNT	3YCNT	TY_01_Y12

19.2 COLOR PATTERN REGISTERS

When the ROP chosen for a BitBLT uses a color pattern, the 8x8 pixel pattern data must be stored in the register address space starting at offset 100 A100H. The amount of register space required is a function of the color depth as shown in Table 19-2. The value is derived by multiplying 64 pixels (8x8 pattern) by the color depth (bytes/pixel) and dividing by 4 bytes/doubleword (32-bit registers).

Table 19-2 Color Pattern Data Storage Requirements

Color Depth (Bits/Pixel)	Storage Requirements (Doublewords)	Offset Range (Hex)
8	16	100 A100 - 100 A13C
16	32	100 A100 - 100 A17C
24	48	100 A100 - 100 A1BC

The pattern color data is written starting with the upper left pixel (0,0) to the end of the line (7,0) and then proceeding across each line to the last pixel (8,8). Pixel 0,0 is written to 100 A100H. The data are stored fully packed.

For 8 bits/pixel, pixel 0,0 is written to the low order byte 0, pixel 1,0 is written to byte 1, etc. Pixel 4,0 would then be written to the low order byte of 100 A104H and so on. The 8-bit value for each pixel is an index to the DAC palette registers.

For 16 bits/pixel, pixel 0,0 is written to the low order word of 100 A100H, pixel 1,0 to the high order word, etc. Either RGB1555 or RGB565 coding can be used.

For 24 bits/pixel, pixel 0,0 is written to the 3 low order bytes of 100 A100H (RGB888 format). The blue value for pixel 1,0 is written to the high order byte of 100 A100H. The red and green values for pixel 1,0 are written to the low order word of 100 A104H and so on. Thus pixel data crosses doubleword boundaries.

19.3 2D REGISTERS

This section describes all the registers used with the 2D drawing commands (BitBLT/Rectangle Fill, 2D Line and 2D Polygon).

Source Base Address Register (SRC_BASE) (MMA4D4, MMA8D4, MMACD4)

Read/Write Offset: A4D4H (BitBLT), A8D4H (2D Line), ACD4H (2D Polygon)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOURCE BASE ADDRESS													0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	SOURCE BASE ADDRESS					

Bits 2-0 Reserved = 0

Bits 21-3 SOURCE BASE ADDRESS

Value = base address in video memory of source data for 2D drawing operations (quadword aligned)

This value is required when the source is video memory (screen). It is different from the destination base address when the data is located in off-screen memory. This is the 0,0 pixel address for off-screen data. The stride for off-screen data is programmed in the Destination/Source Stride register (MMxxE4).

Bits 31-22 Reserved

Destination Base Address Register (DEST_BASE) (MMA4D8, MMA8D8, MMACD8)

Read/Write Offset: A4D8H (BitBLT), A8D8H (2D Line), ACD8H (2D Polygon)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESTINATION BASE ADDRESS													0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	DESTINATION BASE ADDRESS					

Bits 2-0 Reserved = 0

Bits 21-3 DESTINATION BASE ADDRESS

Value = base address in video memory of destination data for 2D drawing operations (quadword aligned)

This is the 0,0 pixel address in video memory for the screen resolution being used. It will normally be at the start of video memory.

Bits 31-22 Reserved

Left/Right Clipping Register (CLIP_L_R) (MMA4DC, MMA8DC, MMACDC)

Read/Write Offset: A4DCH (BitBLT), A8DCH (2D Line), ACDCH (2D Polygon)
Power-On Default: Undefined

Bit 1 of the Command Set register must be set to 1 for the settings in this register to have effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	RIGHT CLIPPING LIMIT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	LEFT CLIPPING LIMIT										

Bits 10-0 RIGHT CLIPPING LIMIT

Value = pixel position of the last pixel to be drawn on each line. The first pixel is 0.

Bits 15-11 Reserved

Bits 26-16 LEFT CLIPPING LIMIT

Value = pixel position of the first pixel to be drawn on each line. The first pixel is 0.

Bits 31-27 Reserved

Top/Bottom Clipping Register (CLIP_T_B) (MMA4E0, MMA8E0, MMACE0)

Read/Write Offset: A4E0H (BitBLT), A8E0H (2D Line), ACE0H (2D Polygon)
Power-On Default: Undefined

Bit 1 of the Command Set register must be set to 1 for the settings in this register to have effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	BOTTOM CLIPPING LIMIT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	TOP CLIPPING LIMIT										

Bits 10-0 BOTTOM CLIPPING LIMIT

Value = line position of the last line to be drawn. The first line is 0.

Bits 15-11 Reserved

Bits 26-16 TOP CLIPPING LIMIT

Value = line position of the first line to be drawn. The first line is 0.

Bits 31-27 Reserved

Destination/Source Stride Register (DEST_SRC_STR) (MMA4E4, MMA8E4, MMACE4)

Read/Write Offset: A4E4H (BitBLT), A8E4H (2D Line), ACE4H (2D Polygon)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	SOURCE STRIDE									0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	DESTINATION STRIDE									0	0	0

Bits 11-0 SOURCE STRIDE

Value = byte offset of vertically adjacent pixels for the source data. Bits 2-0 must be 000b.

Bits 15-12 Reserved

Bits 27-16 DESTINATION STRIDE

Value = byte offset of vertically adjacent pixels for the destination data. Bits 2-0 must be 000b.

Bits 31-28 Reserved

Mono Pattern 0 Register (MONO_PAT_0) (MMA4E8, MMACE8)

Read/Write Offset: A4E8H (BitBLT), ACE8H (2D Polygon)
Power-On Default: Undefined

The pattern data in this register is used when bit 8 of the Command Set register is set to 1 to specify a mono pattern. The first four lines of the pattern are specified in this register.

15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
L20	L21	L22	L23	L24	L25	L26	L27	L10	L11	L12	L13	L14	L15	L16	L17
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
L40	L41	L42	L43	L44	L45	L46	L47	L30	L31	L32	L33	L34	L35	L36	L37

Bits 31-0 MONO PATTERN 0

Value = first (low order) 32 bits of a 64-bit mono pattern

The second (high order) 32 bits are found in the Mono Pattern 1 register. These two registers define an 8x8 mono pattern. In the above register bit table, LXY means bit Y of line X, with the leftmost bit of each line (row) being bit 0.

Mono Pattern 1 Register (MONO_PAT_1) (MMA4EC, MMACEC)

Read/Write Offset: A4ECH (BitBLT), ACECH (2D Polygon)
Power-On Default: Undefined

The pattern data in this register is used when bit 8 of the Command Set register is set to 1 to specify a mono pattern. The second four lines of the pattern are specified in this register.

15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
L60	L61	L62	L63	L64	L65	L66	L67	L50	L51	L52	L53	L54	L55	L56	L57
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
L80	L81	L82	L83	L84	L85	L86	L87	L70	L71	L72	L73	L74	L75	76	L77

Bits 31-0 MONO PATTERN 1

Value = second (high order) 32 bits of a 64-bit mono pattern (little endian format)

The first (low order) 32 bits are found in the Mono Pattern 0 register. These two registers define an 8x8 mono pattern. In the above register bit table, LXY means bit Y of line X, with the leftmost bit of each line (row) being bit 0.

Mono Pattern Background Color Register (PAT_BG_CLR) (MMA4F0, MMACF0)

Read/Write Offset: A4F0H (BitBLT), ACF0H (2D Polygon)
Power-On Default: Undefined

The pattern color data in this register is used when bit 8 of the Command Set register is set to 1 to specify a mono pattern and the pattern bit is 0. The color depth specified must match the value selected by bits 4-2 of the Command Set register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA 2								DATA 1							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	DATA 3							

Bits 7-0 DATA 1

Value = DAC CLUT index (8 bits/pixel), lower byte of color data (15/16 bits/pixel), blue color index (24 bits/pixel

Bits 15-8 DATA 2

Value = Reserved (8 bits/pixel), upper byte of color data (15/16 bits/pixel), green color index (24 bits/pixel)

Bit 23-16 DATA 3

Value = Reserved (8, 15 or 16 bits/pixel), red color index (24 bits/pixel)

Bits 31-24 Reserved

Mono Pattern Foreground Color Register (PAT_FG_CLR) (MMA4F4, MMA8F4, MMACF4)

Read/Write Offset: A4F4H (BitBLT), A8F4H (2D Line), ACF4H (2D Polygon)
Power-On Default: Undefined

The pattern color data in this register is used when bit 8 of the Command Set register is set to 1 to specify a mono pattern and the pattern bit is 1. It is also the pattern color used for rectangle fills, line draws and polygon fills, regardless of any pattern specification. The color depth specified must match the value selected by bits 4-2 of the Command Set register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA 2								DATA 1							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	DATA 3							

Bits 7-0 DATA 1

Value = DAC CLUT index (8 bits/pixel), lower byte of color data (15/16 bits/pixel), blue color index (24 bits/pixel

Bits 15-8 DATA 2

Value = Reserved (8 bits/pixel), upper byte of color data (15/16 bits/pixel), green color index (24 bits/pixel)

Bit 23-16 DATA 3

Value = Reserved (8, 15 or 16 bits/pixel), red color index (24 bits/pixel)

Bits 31-24 Reserved

Source Background Color Register (SRC_BG_CLR) (MMA4F8)

Read/Write Offset: A4F8H (BitBLT)
Power-On Default: Undefined

For mono image transfers (bit 6 of the Command Set register set to 1), this is the source color when the image bit is 0. It is not used when color compare is enabled (bit 9 of the Command Set register set to 1). The color depth specified must match the value selected by bits 4-2 of the Command Set register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA 2								DATA 1							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	DATA 3							

Bits 7-0 DATA 1

Value = DAC CLUT index (8 bits/pixel), lower byte of color data (15/16 bits/pixel), blue color index (24 bits/pixel

Bits 15-8 DATA 2

Value = Reserved (8 bits/pixel), upper byte of color data (15/16 bits/pixel), green color index (24 bits/pixel)

Bit 23-16 DATA 3

Value = Reserved (8, 15 or 16 bits/pixel), red color index (24 bits/pixel)

Bits 31-24 Reserved

Source Foreground Color Register (SRC_FG_CLR) (MMA4FC)

Read/Write Offset: A4FCH (BitBLT)
Power-On Default: Undefined

For mono image transfers (bit 6 of the Command Set register set to 1), this is the source color when the image bit is 1. For 8- or 15/16-bits/pixel color image transfers when transparent color is enabled (bit 9 of the Command Set register set to 1), the image data color is compared with this color. If it matches, the screen is not updated. If it does not match, the image data color is used to update the screen. In all cases, the color depth specified must match the value selected by bits 4-2 of the Command Set register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA 2								DATA 1							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	DATA 3							

Bits 7-0 DATA 1

Value = DAC CLUT index (8 bits/pixel), lower byte of color data (15/16 bits/pixel), blue color index (24 bits/pixel)

The 24 bits/pixel color is used only for mono image transfers.

Bits 15-8 DATA 2

Value = DAC CLUT index (8 bits/pixel), upper byte of color data (15/16 bits/pixel), green color index (24 bits/pixel)

The 8 bits/pixel color must be programmed to both the DATA 1 and DATA 2 bytes. The 24 bits/pixel color is used only for mono image transfers.

Bit 23-16 DATA 3

Value = Reserved (8, 15 or 16 bits/pixel), red color index (24 bits/pixel)

This color is used only for mono image transfers.

Bits 31-24 Reserved

Command Set Register (CMD_SET) (MMA500, MMA900, MMAD00)

Read/Write Offset: A500H (BitBLT), A900H (2D Line), AD00H (2D Polygon)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	FDO		ITA		TP	MP	IDS	MS	DE	DEST FORMAT			HC	AE
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
23D	2D COMMAND				YP	XP	256 ROPS								R

Bit 0 AE - Autoexecute
0 = Execute command when this register is written to
1 = Execute command when the highest address register in a drawing type set is written to

The highest address register in a drawing type set is easily seen in Table 19-1, where it is the bottom register in each column. For example, if this bit is set to 1, a BitBLT is executed when the RDEST_XY (MMA50C) register is written to. Similarly, execution of a 2D line command is based on writing to the LYCNT register, etc. This setting allows multiple executions of a given command using different parameters without rewriting the Command Set register.

To turn off autoexecute without executing a command, write to this register with this bit cleared to 0 and bits 30-27 programmed to 1111b (NOP).

Bit 1 HC - Hardware Clipping Enable
0 = Hardware clipping disabled
1 = Hardware clipping enabled

The settings in the clipping registers (MMxxDC, MMxxE0) are effective only when this bit is set to 1.

Bits 4-2 DEST FORMAT - Destination Color Format
000 = 8 bits/pixel palettized
001 = 16 bits/pixel (RGB1555 or RGB565)
010 = 24 bits/pixel, RGB888

All other values are reserved.

Bit 5 DE - Draw Enable
0 = Don't update screen
1 = Update screen (normal draw)

Parameter values calculated during the execution of the command end up the same regardless of the setting of this bit. That is, the command is fully executed except for the possible non-drawing of the new pixel.

Bit 6 MS - Mono Source (Image Transfers)
0 = Source data is the same pixel depth as the destination data
1 = Source data is mono

Bit 7 IDS - Image Data Source
0 = Source data is from video memory (screen)
1 = Source data is from the image transfer port (CPU, system memory)

When this bit is set to 1, source data is provided by CPU writes to the offset range of 100 0000H to 100 7FFFH. Bit 6 of this register specifies whether mono or color data is being transferred.

Bit 8 MP - Mono Pattern
0 = Pattern data is the same pixel depth as the destination data
1 = Pattern data is mono

This bit is cleared to 0 for a BitBLT using a ROP with a color source. The 8x8 color pattern is found starting at location 100 A100H. For a mono pattern, the pattern information is determined from the Mono Pattern 0 and 1 registers. This bit must be set to 1 for a rectangle fill operation.

Bit 9 TP - Transparent
0 = A mono source image transfer uses both the source foreground (image bit = 1) and source background (image bit = 0) colors to update the screen. A color image transfer uses the CPU-provided colors.
1 = A mono source image transfer updates the screen only when the source foreground color is selected (image bit = 1). Otherwise (image bit = 0), the screen pixel is left unchanged. A color image transfer updates the screen with the transmitted color only when that color does not match the color in the source foreground color register. If a color match occurs, the destination pixel is not updated. This transparent color feature for color image transfers can be used for 8- and 16-bit color modes, but not for 24-bit color.

Note: This bit is effective only when bit 7 of this register is set to 1. A setting of 1 for the mono source case provides “transparent text” capability. The term “transparent text” refers to the updating of only the pixels forming the text characters and not the entire rectangular text block using the background color for non-text areas.

Bits 11-10 ITA - Image Transfer Alignment
00 = Data for each line of an image transfer is byte aligned
01 = Data for each line of an image transfer is word aligned
10 = Data for each line of an image transfer is doubleword aligned
11 = Reserved

All image transfers are doublewords. If the end of a bit map line is reached within a doubleword transfer, the setting of these bits determines how the start of the next line is handled. If doubleword aligned, data in the last doubleword beyond the end of the line is discarded and the next line begins on the next doubleword. If word aligned and an upper word of data remains after the end of the line is reached, that word will be used to begin the next line. If byte aligned, the next line with begin on the next byte in the doubleword after the end of the line. The latter is used only for mono source data, e.g., text.

Bits 13-12 FDO - First Doubleword Offset (Image Transfers)
00 = Entire first doubleword of an image transfer contains valid data
01 = Start with the second byte of the first doubleword of an image transfer
10 = Start with the third byte of the first doubleword of an image transfer
11 = Start with the fourth byte of the first doubleword of an image transfer

Bits 16-14 Reserved

Bits 24-17 256 ROPS - 256 Raster Operations

Value = binary key selecting one of 256 three operand raster operations as defined in Appendix A.

The full 256 three-operand ROPs are available for BitBLT and image transfer operations. The other 2D operations (Rectangle Fill, Line Draw and Polygon Fill) can only use the subset of the 256 ROPs that does not have a source. When the ROP contains a pattern, the pattern must be mono and the hardware forces the pattern value to the pattern foreground color regardless of the values programmed in the Mono Pattern registers.

Bit 25 XP - X Positive (BitBLT)
0 = A BitBLT is performed from right to left (X negative)
1 = A BitBLT is performed from left to right (X positive)

Bit 26 YP - Y Positive (BitBLT)
0 = A BitBLT is performed from bottom to top (Y negative)
1 = A BitBLT is performed from top to bottom (Y positive)

Bits 30-27 2D COMMAND
0000 = BitBLT
0001 = Reserved
0010 = Rectangle Fill
0011 = Line Draw
0100 = Reserved
0101 = Polygon Fill
0110 = Reserved
0111 = Reserved
1000 = Reserved
1001 = Reserved
1010 = Reserved
1011 = Reserved
1100 = Reserved
1101 = Reserved
1110 = Reserved
1111 = NOP

The NOP option is required to turn off autoexecute without executing a command. See the definition for bit 0 of this register.

Bit 31 23D - 2D or 3D Select
0 = A 2D command is being executed
1 = A 3D command is being executed

Rectangle Width/Height Register (RWIDTH_HEIGHT) (MMA504)

Read/Write Offset: A504H (BitBLT)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	RECTANGLE HEIGHT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	RECTANGLE WIDTH										

Bits 10-0 RECTANGLE HEIGHT

Value = height in lines of the rectangle to be drawn or blitted

A value of 1 equals 1 line.

Bits 15-11 Reserved

Bits 26-16 RECTANGLE WIDTH

Value = width in pixels of the rectangle to be drawn or blitted

A value of 0 equals 1 pixel/line.

Bits 31-27 Reserved

Rectangle Source XY Register (RSRC_XY) (MMA508)

Read/Write Offset: A508H (BitBLT)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SOURCE Y										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	SOURCE X										

Bits 10-0 SOURCE Y

Value = y coordinate in lines of the upper left hand corner of the source rectangle for a BitBLT

Bits 15-11 Reserved

Bits 26-16 SOURCE X

Value = x coordinate in pixels of the upper left hand corner of the source rectangle for a BitBLT

Bits 31-27 Reserved

Note: The starting coordinate is 0,0.

Rectangle Destination XY Register (RDEST_XY) (MMA50C)

Read/Write Offset: A50CH (BitBLT)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	DESTINATION Y										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	DESTINATION X										

Bits 10-0 DESTINATION Y

Value = y coordinate in lines of the upper left hand corner of the filled rectangle to be drawn or the destination for a BitBLT

Bits 15-11 Reserved

Bits 26-16 DESTINATION X

Value = x coordinate in pixels of the upper left hand corner of the filled rectangle to be drawn or the destination for a BitBLT

Bits 31-27 Reserved

Note: The starting coordinate is 0,0.

Line Draw Endpoints Register (LXEND0_END1) (MMA96C)

Read/Write Offset: A96CH (2D Line)
Power-On Default: Undefined

This register specifies the x coordinates of the first and last pixels drawn for a line. This provides the ability to not draw the last pixel of each line segment when the line is to be extended to form a polyline.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	END1										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	0	0	0	0	END0										

Bits 15-0 END1

Value = x coordinate (in pixels) of the last pixel to be drawn for the topmost scanline. The first coordinate value is 0. Bits 15-11 are sign bits and must be 0's to indicate a positive value.

Bits 31-16 END0

Value = x coordinate (in pixels) of the first pixel to be drawn for the bottommost scanline. The first coordinate value is 0. Bits 31-27 are sign bits and must be 0's to indicate a positive value.

ViRGE line draw always proceeds from bottom to top. If the requested line is drawn upward with a don't draw the last pixel instruction, the END0 coordinate will be the same as the requested start x coordinate and the END1 coordinate will be 1 less (if drawn from left to right) or 1 more (if drawn from right to left) than the requested end x coordinate. If the requested line is drawn downward, the END1 coordinate will be the same as the requested start x coordinate and the END0 coordinate will be 1 more (if drawn from right to left) or one less (if drawn from left to right) than the requested end x coordinate. See the programming examples for 2D line draw for a more detailed explanation.

Line Draw X Delta Register (LdX) (MMA970)

Read/Write Offset: A970H (2D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
X DELTA HIGH															

Bits 31-0 X DELTA

Value = - (ΔX << 20)/ΔY) with integer division

If the requested line is from coordinates x1,y1 to x2,y2, ΔX is x2 - x1 and ΔY is y2 - y1. (ΔX = x1 - x2 and ΔY = y1 - y2 also works.) The field format is S11.20, i.e, bit 31 is the sign bit (0 = positive), with 11 integer positions and 20 fractional positions.

Line Draw X Start Register (LXSTART) (MMA974)

Read/Write Offset: A974H (2D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X START LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
X START HIGH															

Bits 31-0 X START

For an X major line, + X DELTA, value = (x1 << 20) + (X DELTA/2)
For an X major line, - X DELTA, value = (x1 << 20) + (X DELTA/2) + ((1 << 20) - 1)
For a Y major line, value = x1 << 20

For an X major line, the absolute x value increases faster than the absolute y value as the line is drawn. In this case, there may be more than one pixel drawn per scan line. For a Y major line, the absolute y value increases faster than the absolute x value. In this case, at most one pixel will be drawn per scan line. If the requested line is drawn upward, x1 is the requested starting x coordinate. If the requested line is drawn downward, x1 is the requested ending x coordinate. X DELTA is the value programmed in MMA970. The field format is S11.20, i.e, bit 31 is the sign bit (0 = positive), with 11 integer positions and 20 fractional positions.

Line Draw Y Start Register (LYSTART) (MMA978)

Read/Write Offset: A978H (2D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	Y START										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 Y START

Value = Y coordinate (in scan lines) of first scan line to be drawn

ViRGE draws lines from bottom to top. Therefore this value will be the largest of the requested starting and ending y coordinates.

Bits 31-11 Reserved

Line Draw Y Count Register (LYCNT) (MMA97C)

Read/Write Offset: A97CH (2D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SCAN LINE COUNT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DIR	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 SCAN LINE COUNT

Value = [abs (y2 - y1)] +1

y2 is the requested ending y coordinate and y1 is the requested starting y coordinate.

Bits 30-11 Reserved

Bit 31 DIR - Drawing Direction
0 = Draw line from right to left
1 = Draw line from left to right

Polygon Right X Delta Register (PRDX) (MMAD68)

Read/Write Offset: AD68H (Polygon Fill)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RIGHT EDGE X DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RIGHT EDGE X DELTA HIGH															

Bits 31-0 RIGHT EDGE X DELTA

Value = - (ΔX << 20)/ΔY) with integer division

If the requested line is from coordinates x1,y1 to x2,y2, ΔX is x2 - x1 and ΔY is y2 - y1. (ΔX = x1 - x2 and ΔY = y1 - y2 also works.) The field format is S11.20, i.e, bit 31 is the sign bit (0 = positive), with 11 integer positions and 20 fractional positions.

Polygon Right X Start Register (PRXSTART) (MMAD6C)

Read/Write Offset: AD6CH (Polygon Fill)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RIGHT EDGE X START LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RIGHT EDGE X START HIGH															

Bits 31-0 RIGHT EDGE X START

For an X major line, value = (x1 << 20) - (RIGHT EDGE X DELTA/2) + (1 << 19)
For a Y major line, value = x1 << 20 + (1 << 19)

For an X major line, the absolute x value increases faster than the absolute y value as the line is drawn. In this case, there may be more than one pixel drawn per scan line. For a Y major line, the absolute y value increases faster than the absolute x value. In this case, at most one pixel will be drawn per scan line. If the requested line is drawn upward, x1 is the requested starting x coordinate. If the requested line is drawn downward, x1 is the requested ending x coordinate. X DELTA is the value programmed in MMA970. The field format is S11.20, i.e, bit 31 is the sign bit (0 = positive), with 11 integer positions and 20 fractional positions.

Polygon Left X Delta Register (PLDX) (MMAD70)

Read/Write Offset: AD70H (Polygon Fill)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEFT EDGE X DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LEFT EDGE X DELTA HIGH															

Bits 31-0 LEFT EDGE X DELTA

Value = - (ΔX << 20)/ΔY) with integer division

If the requested line is from coordinates x1,y1 to x2,y2, ΔX is x2 - x1 and ΔY is y2 - y1. (ΔX = x1 - x2 and ΔY = y1 - y2 also works.) The field format is S11.20, i.e, bit 31 is the sign bit (0 = positive), with 11 integer positions and 20 fractional positions.

Polygon Left X Start Register (PLXSTART) (MMAD74)

Read/Write Offset: AD74H (Polygon Fill)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEFT EDGE X START LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LEFT EDGE X START HIGH															

Bits 31-0 LEFT EDGE X START

For an X major line, value = (x1 << 20) - (LEFT EDGE X DELTA/2) + (1 << 19)
For a Y major line, value = x1 << 20 + (1 << 19)

For an X major line, the absolute x value increases faster than the absolute y value as the line is drawn. In this case, there may be more than one pixel drawn per scan line. For a Y major line, the absolute y value increases faster than the absolute x value. In this case, at most one pixel will be drawn per scan line. If the requested line is drawn upward, x1 is the requested starting x coordinate. If the requested line is drawn downward, x1 is the requested ending x coordinate. X DELTA is the value programmed in MMA970. The field format is S11.20, i.e, bit 31 is the sign bit (0 = positive), with 11 integer positions and 20 fractional positions.

Polygon Y Start Register (PYSTART) (MMAD78)

Read/Write Offset: AD78H (Polygon Fill)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	Y START										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 Y START

Value = Y coordinate (in scan lines) of first scan line to be drawn

ViRGE draws lines from bottom to top. Therefore this value will be the largest of the requested starting and ending y coordinates. This value need only be programmed once for each polygon.

Bits 31-11 Reserved

Polygon Y Count Register (PYCNT) (MMAD7C)

Read/Write Offset: AD7CH (Polygon Fill)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SCAN LINE COUNT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	ULE	URE	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 SCAN LINE COUNT

Value = [abs (y2 - y1] +1

The first polygon update proceeds upward to the first vertex. y2 is the requested ending y coordinate for the line leading to that vertex and y1 is the requested starting y coordinate for that line. Both bit 28 and bit 29 will be set to 1 for the first update. For the second polygon update, only the X DELTA for the line extending from the first vertex is re-specified and only the update bit (28 or 29) for that edge is set to 1. The value in this scan line count field is set for the number of scan lines from the first vertex to the second vertex. See the polygon fill programming examples for a more complete explanation of how to program the polygon fill registers at each step to form a complete polygon.

Bits 27-11 Reserved

Bit 28 URE - Update Right Edge
0 = Do not update right edge
1 = Update right edge

Bit 29 ULE - Update Left Edge
0 = Do not update left edge
1 = Update left edge

Bits 31-30 Reserved

19.4 3D REGISTERS

Z-Buffer Base Address Register (Z_BASE) (MMB0D4, MMB4D4)

Read/Write Offset: B0D4H (3D Line), B4D4H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z-BUFFER BASE ADDRESS													0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	Z-BUFFER BASE ADDRESS					

Bits 2-0 Reserved = 0

Bits 21-3 Z-BUFFER BASE ADDRESS

Value = base address in video memory of the z-buffer used in 3D drawing operations to store depth information for each pixel. Bits 2-0 must be 000b (quadword aligned).

Bits 31-22 Reserved

Destination Base Address Register (DEST_BASE) (MMB0D8, MMB4D8)

Read/Write Offset: B0D8H (3D Line), B4D8H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESTINATION BASE ADDRESS													0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	DESTINATION BASE ADDRESS					

Bits 2-0 Reserved = 0

Bits 21-3 DESTINATION BASE ADDRESS

Value = base address in video memory of destination data for 2D drawing operations. Bits 2-0 must be 000b (quadword aligned).

This is the 0,0 pixel address in video memory for the screen resolution being used. It will normally be at the start of video memory.

Bits 31-22 Reserved

Left/Right Clipping Register (CLIP_L_R) (MMB0DC, MMB4DC)

Read/Write Offset: B0DCH (3D Line), B4DCH (3D Triangle)
Power-On Default: Undefined

Bit 1 of the Command Set register must be set to 1 for the settings in this register to have effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	RIGHT CLIPPING LIMIT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	LEFT CLIPPING LIMIT										

Bits 10-0 RIGHT CLIPPING LIMIT

Value = pixel position of the last pixel to be drawn on each line. The first pixel is 0.

Bits 15-11 Reserved

Bits 26-16 LEFT CLIPPING LIMIT

Value = pixel position of the first pixel to be drawn on each line. The first pixel is 0.

Bits 31-27 Reserved

Top/Bottom Clipping Register (CLIP_T_B) (MMB0E0, MMB4E0)

Read/Write Offset: B0E0H (3D Line), B4E0H (3D Triangle)
Power-On Default: Undefined

Bit 1 of the Command Set register must be set to 1 for the settings in this register to have effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	BOTTOM CLIPPING LIMIT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	TOP CLIPPING LIMIT										

Bits 10-0 BOTTOM CLIPPING LIMIT

Value = line position of the last line to be drawn. The first line is 0.

Bits 15-11 Reserved

Bits 26-16 TOP CLIPPING LIMIT

Value = line position of the first line to be drawn. The first line is 0.

Bits 31-27 Reserved

Destination/Source Stride Register (DEST_SRC_STR) (MMB0E4, MMB4E4)

Read/Write Offset: B0E4H (3D Line), B4E4H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	SOURCE STRIDE										0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	DESTINATION STRIDE										0	0	0

Bits 12-0 SOURCE STRIDE (3D Triangle only)

Value = byte offset of vertically adjacent pixels for a flat (not mipmapped) texture map. Bits 2-0 must be 000b. **Bit 12 (MSB) is available only for chip revision AC and later.**

Bits 15-12 Reserved

Bits 28-16 DESTINATION STRIDE

Value = byte offset of vertically adjacent pixels for the destination data. Bits 2-0 must be 000b. **Bit 28 (MSB) is available only for chip revision AC and later.**

Bits 31-28 Reserved

Z Stride Register (Z_STRIDE) (MMB0E8, MMB4E8)

Read/Write Offset: B0E8H (3D Line), B4E8H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	Z STRIDE										0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 11-0 Z STRIDE

Value = byte offset of vertically adjacent pixels for the Z-buffer data . Bits 2-0 must be 000b. **Bit 12 (MSB) is available only for chip revision AC and later.**

Z-buffer data is always 16 bits/pixel. If the destination format is 16 bits/pixel, the Z stride will be the same as the destination stride. Otherwise, the Z stride will differ from the destination stride according to the differing pixel depths.

Bits 31-12 Reserved

Texture Base Address Register (TEX_BASE) (MMB4EC)

Read/Write Offset: B4ECH (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEXTURE BASE ADDRESS													0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	TEXTURE BASE ADDRESS					

Bits 2-0 Reserved = 0

Bits 21-3 TEXTURE BASE ADDRESS

Value = base address in video memory of the texture data (flat or mipmapped). Bits 2-0 must be 000b (quadword aligned).

Bits 31-22 Reserved

Texture Border Color Register (TEX_BDR_CLR) (MMB4F0)

Read/Write Offset: B4F0H (3D Triangle)
Power-On Default: Undefined

This is used as the texel color for lighting when texture wrapping is not enabled (bit 26 of the Command Set register is cleared to 0) and the texture rectangle is too small to complete the fill. This must be in the same format at the texture color.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA 2								DATA 1							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	DATA 3							

Bits 7-0 DATA 1

Value = DAC CLUT index (8 bits/pixel), lower byte of color data (15/16 bits/pixel), blue color index (24 bits/pixel

Bits 15-8 DATA 2

Value = Reserved (8 bits/pixel), upper byte of color data (15/16 bits/pixel), green color index (24 bits/pixel)

Bit 23-16 DATA 3

Value = Reserved (8, 15 or 16 bits/pixel), red color index (24 bits/pixel)

Bits 31-24 Reserved

Fog Color Register (FOG_CLR) (MMB0F4, MMB4F4)

Read/Write Offset: B0F4H (3D Line), B0F4H (3D Triangle)
Power-On Default: Undefined

This is the fog color blended with the pixel color when bit 17 of the Command Set register is set to 1. This operation is also called depth cueing when the fog factor (source alpha) corresponds to the distance from the viewer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN COLOR INDEX								BLUE COLOR INDEX							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	RED COLOR INDEX							

Bits 7-0 BLUE COLOR INDEX

Bits 15-8 GREEN COLOR INDEX

Bit 23-16 RED COLOR INDEX

Bits 31-24 Reserved

Color0 Register (COLOR0) (MMB4F8)

Read/Write Offset: B4F8H (3D Triangle)
Power-On Default: Undefined

When using one of the Blend4 modes for texel storage, this register specifies one of the color limits used in the interpolation of the texel color during the generate phase of pixel coloring.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN COLOR INDEX								BLUE COLOR INDEX							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	RED COLOR INDEX							

Bits 7-0 BLUE COLOR INDEX

Bits 15-8 GREEN COLOR INDEX

Bit 23-16 RED COLOR INDEX

Bits 31-24 Reserved

Color1 Register (COLOR1) (MMB4FC)

Read/Write Offset: B4FCH (3D Triangle)
Power-On Default: Undefined

When using one of the Blend4 modes for texel storage, this register specifies one of the color limits used in the interpolation of the texel color during the generate phase of pixel coloring.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN COLOR INDEX								BLUE COLOR INDEX							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	RED COLOR INDEX							

Bits 7-0 BLUE COLOR INDEX

Bits 15-8 GREEN COLOR INDEX

Bit 23-16 RED COLOR INDEX

Bits 31-24 Reserved

Command Set Register (CMD_SET) (MMB100, MMB500)

Read/Write Offset: B100H (3D Line), B500H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TB	TEX FLTR MODE			MIPMAP LEVEL SIZE				TEX CLR FORMAT			DEST FORMAT			HC	AE
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
23D	3D COMMAND				TWE	ZB MODE		ZUP	ZB COMP			ABC		FE	TB

Bit 0 AE - Autoexecute
0 = Execute command when this register is written to
1 = Execute command when the highest address register in a drawing type set is written to

The highest address register in a drawing type set is easily seen in Table 19-1, where it is the bottom register in each column. For example, if this bit is set to 1, a 3D line is executed when the 3YCNT (MMB17C) register is written to. Similarly, execution of a 3D Triangle command is based on writing to the TY01_Y12 (MMB57C) register. This setting allows multiple executions of a given command using different parameters without re-writing the Command Set register.

To turn off autoexecute without executing a command, write to this register with this bit cleared to 0 and bits 30-27 programmed to 1111b (NOP).

Bit 1 HC - Hardware Clipping Enable
0 = Hardware clipping disabled
1 = Hardware clipping enabled

The settings in the clipping registers (MMxxDC, MMxxE0) are effective only when this bit is set to 1.

Bits 4-2 DEST FORMAT - Destination Color Format
000 = 8 bits/pixel palettized
001 = 16 bits/pixel (ZRGB1555)
010 = 24 bits/pixel, RGB888

All other values are reserved.

Bits 7-5 TEX CLR FORMAT - Texel Color Format
000 = 32 bits/pixel (ARGB8888)
001 = 16 bits/pixel (ARGB4444)
010 = 16 bits/pixel (ARGB1555)
011 = 8 bits/pixel (Alpha4, Blend4)
100 = 4 bits/pixel (Blend4, low nibble)
101 = 4 bits/pixel (Blend4, high nibble)
110 = 8 bits/pixel (palettized)
111 = YU/YV (16 bits/pixel equivalent)

Bits 11-8 MIPMAP LEVEL SIZE

Value = s, where 2^s is the size of one side of the largest mipmap texture rectangle

For example, a value of 4 specifies the largest mipmap as 2^4 x 2^4 = 16 x 16 texels. The largest allowable s value is 9, which specifies a 512 x 512 texel texture.

Bits 14-12 TEX FLTR MODE - Texture Filtering Mode
000 = M1TPP (MIP_NEAREST)
001 = M2TPP (LINEAR_MIP_NEAREST)
010 = M4TPP (MIP_LINEAR)
011 = M8TPP (LINEAR_MIP_LINEAR)
100 = 1TPP (NEAREST)
101 = Fast Bilinear
110 = 4TPP (LINEAR)
111 = Reserved

Only modes with no filtering (000b and 100b) can be used with 8 bits/pixel palettized data. In addition, the texture blending mode must be decal (bits 16-15 of this register = 10b.)

Bits 16-15 TB - Texture Blending Mode
00 = Complex Reflection
01 = Modulate
10 = Decal
11 = Reserved

Bit 17 FE - Fog Enable
0 = Fog color blending disabled
1 = Fog color blending enabled

Fogging is not available for Gouraud shaded triangles or if source alpha is used for blending. If the fog factor (source pixel alpha value) corresponds to the distance from the viewer, this function is also called depth cueing.

Bits 19-18 ABC - Alpha Blending Control
00 = No alpha blending
01 = No alpha blending
10 = Use texture alpha for blending
11 = Use source alpha for blending

Bits 22-20 ZB COMP - Z-buffer Compare Mode
000 = z compare never passes
001 = Pass if Zs > Zzb
010 = Pass if Zs = Zzb
011 = Pass if Zs ≥ Zzb
100 = Pass if Zs < Zzb
101 = Pass if Zs ≠ Zzb
110 = Pass if Zs ≤ Zzb
111 = z compare always passes

Bit 23 ZUP - Z Update Enable
0 = Never update z-buffer
1 = Update z-buffer with new (source) pixel z value if the z compare passes

Bits 25-24 ZB MODE - Z-buffering Mode
00 = Normal Z-buffering
01 = MUX buffering (Z-buffer pass)
10 = MUX buffering (draw buffer pass)
11 = No Z-buffering

Bit 26 TWE - Texture Wrap Enable
0 = Texture wrapping disabled
1 = Texture wrapping enabled

If wrapping is disabled, the texture border color (MMB4F0) may need to be specified. This bit is reserved if MMB508_31 = 1.

Bits 30-27 3D COMMAND
0000 = Gouraud Shaded Triangle
0001 = Lit Texture Triangle. Reserved if MMB508_31 = 1
0010 = Unlit Texture Triangle. Reserved if MMB508_31 = 1
0011 = Reserved
0100 = Reserved
0101 = Lit Texture Triangle with perspective
0110 = Unlit Texture Triangle with perspective
0111 = Reserved
1000 = 3D Line
1001 = Reserved
1010 = Reserved
1011 = Reserved
1100 = Reserved
1101 = Reserved
1110 = Reserved
1111 = NOP

The NOP option is required to turn off autoexecute without executing a command. See the definition for bit 0 of this register.

Bit 31 23D - 2D or 3D Select
0 = A 2D command is being executed
1 = A 3D command is being executed

3D Line Draw GB Delta Register (3dGdY_dBdY) (MMB144)

Read/Write Offset: B144H (3D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLUE DELTA															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GREEN DELTA															

Bits 15-0 BLUE DELTA

Value = Delta value for the accumulation of the blue attribute. The format is S8.7.

Bits 31-16 GREEN DELTA

Value = Delta value for the accumulation of the green attribute. The format is S8.7.

3D Line Draw AR Delta Register (3dAdY_dRdY) (MMB148)

Read/Write Offset: B148H (3D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED DELTA															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ALPHA DELTA															

Bits 15-0 RED DELTA

Value = Delta value for the accumulation of the red attribute. The format is S8.7.

Bits 31-16 ALPHA DELTA

Value = Delta value for the accumulation of the alpha attribute. The format is S8.7.

3D Line Draw GB Start Register (3GS_BS) (MMB14C)

Read/Write Offset: B14CH (3D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	BLUE START														
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	GREEN START														

Bits 15-0 BLUE START

Value = Starting value for the accumulation of the blue attribute. The format is S8.7, where S must be 0.

Bits 31-16 GREEN START

Value = Starting value for the accumulation of the green attribute. The format is S8.7, where S must be 0.

3D Line Draw AR Start Register (3AS_RS) (MMB150)

Read/Write Offset: B150H (3D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RED START														
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	ALPHA START														

Bits 15-0 RED START

Value = Starting value for the accumulation of the red attribute. The format is S8.7, where S must be 0.

Bits 31-16 ALPHA START

Value = Starting value for the accumulation of the alpha attribute. The format is S8.7, where S must be 0.

3D Line Draw Z Delta Register (3dZ) (MMB158)

Read/Write Offset: B158H (3D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Z DELTA HIGH															

Bits 31-0 Z DELTA

Value = Delta value for the accumulation of the Z attribute. The format is S16.15.

3D Line Draw Z Start Register (3ZSTART) (MMB15C)

Read/Write Offset: B15CH (3D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z START LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	Z START HIGH														

Bits 31-0 Z START

Value = Starting value for the accumulation of the Z attribute. The format is S16.15, where S must be 0.

3D Line Draw Endpoints Register (3XEND0_END1) (MMB16C)

Read/Write Offset: B16CH (3D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	END1										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	0	0	0	0	END0										

Bits 15-0 END1

Value = x coordinate (in pixels) of the last pixel to be drawn for the topmost scanline. The first coordinate value is 0. Bits 15-11 are sign bits and must be 0's to indicate a positive value.

Bits 31-16 END0

Value = x coordinate (in pixels) of the first pixel to be drawn for the bottommost scanline. The first coordinate value is 0. Bits 31-27 are sign bits and must be 0's to indicate a positive value.

3D Line Draw X Delta Register (3dX) (MMB170)

Read/Write Offset: B170H (3D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
X DELTA HIGH															

Bits 31-0 X DELTA

Value = Delta value for the accumulation of the X attribute. The format is S11.20.

3D Line Draw X Start Register (3XSTART) (MMB174)

Read/Write Offset: B174H (3D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X START LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	X START HIGH														

Bits 31-0 X START

Value = Starting value for the accumulation of the X attribute. The format is S11.20, where S must be 0.

3D Line Draw Y Start Register (3YSTART) (MMB178)

Read/Write Offset: B178H (3D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	Y START										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 Y START

Value = Y coordinate (in scan lines) of first scan line to be drawn

ViRGE draws lines from bottom to top. Therefore this value will be the largest of the requested starting and ending y coordinates.

Bits 31-11 Reserved

3D Line Draw Y Count Register (3YCNT) (MMB17C)

Read/Write Offset: AB1CH (3D Line)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SCAN LINE COUNT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DIR	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 SCAN LINE COUNT

Value = The number of scan lines to be rendered

Bits 30-11 Reserved

Bit 31 DIR - Drawing Direction
0 = Draw line from right to left
1 = Draw line from left to right

Triangle Base V Register (TBV) (MMB504)

Read/Write Offset: B504H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE V															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
L0 CONSTANT										R	R	BASE V			

Bits 19-0 BASE V

Value = Base vertical coordinate value for texels. The format is (4 + s).(16-s), where s is the number of mipmap levels programmed in MMB500_11-8.

This is the common offset for all V coordinate values for textures. When MMB508_31 = 1, the format of this field remains the same, but the upper 4 bits (19-16) are always 0000b and the fractional bits (16- s) are always 0's.

Bits 21-20 Reserved

Bits 31-22 L0 CONSTANT

Value = L0 constant for the log D calculation.

This field is effective only when MM8508_31 = 1. Otherwise, it is reserved.

Triangle Base U Register (TBU) (MMB508)

Read/Write Offset: B508H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE U															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S3d MODE			R	R	R	R	R	R	R	R	R	BASE U			

Bits 19-0 BASE U

Value = Base horizontal coordinate value for texels. The format is (4 + s).(16-s), where s is the number of mipmap levels programmed in MMB500_11-8.

This is the common offset for all U coordinate values for textures. When MMB508_31 = 1, the format of this field remains the same, but the upper 4 bits (19-16) are always 0000b and the fractional bits (16- s) are always 0's.

Bits 28-20 Reserved

Bits 31-29 S3d Mode
0xx = Original S3d mode (compatible with original S3d engine software)
100 = Extended S3d mode without D change
101 = Extended S3d mode: L0 - (fastlog2 D)
110 = Extended S3d mode: L0 - (2 * fastlog2 D)
111 = Extended S3d mode: L0 - (1.5 * fastlog2 D)

Triangle WX Delta Register (TdWdX) (MMB50C)

Read/Write Offset: B50CH (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WX DELTA LOW															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WX DELTA HIGH															

Bits 31-0 WX DELTA

Value = Delta value for the accumulation of the W attribute (homogeneous coordinate) with respect to X. The format is S12.19.

W is the depth coordinate for 3D texture maps.

Triangle WY Delta Register (TdWdY) (MMB510)

Read/Write Offset: B510H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WY DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WY DELTA HIGH															

Bits 31-0 WY DELTA

Value = Delta value for the accumulation of the W attribute (homogeneous coordinate) with respect to Y. The format is S12.19.

W is the depth coordinate for 3D texture maps.

Triangle W Start Register (TWS) (MMB514)

Read/Write Offset: B514H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W START LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	W START HIGH														

Bits 31-0 W START

Value = Starting value for the accumulation of the W attribute (homogeneous coordinate). The format is S12.19, where S must be 0.

W is the depth coordinate for 3D texture maps.

Triangle DX Delta Register (TdDdX) (MMB518)

Read/Write Offset: B518H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DX DELTA LOW															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DX DELTA HIGH															

Bits 31-0 DX DELTA

Value = Delta value for the accumulation of the D attribute with respect to X. The format is S4.27.

Triangle VX Delta Register (TdVdX) (MMB51C)

Read/Write Offset: B51CH (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VX DELTA LOW															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VX DELTA HIGH															

Bits 31-0 VX DELTA

Value = Delta value for the accumulation of the V attribute with respect to X. The format is S(4 + s).(27 - s) if perspective is enabled (3D command = 0101b or 0110b), where s is the number of mipmap levels programmed in MMB500_11-8. The format is S12.8.11 without perspective enabled. This format is 1 sign bit, 12 integer bits, 8 filter bits and 11 fractional bits.

When MM8508_31 = 1, the format changes to S23.8.

Triangle UX Delta Register (TdUdX) (MMB520)

Read/Write Offset: B520H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UX DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
UX DELTA HIGH															

Bits 31-0 UX DELTA

Value = Delta value for the accumulation of the U attribute with respect to X. The format is S(4 + s).(27 - s) if perspective is enabled (3D command = 0101b or 0110b), where s is the number of mipmap levels programmed in MMB500_11-8. The format is S12.8.11 without perspective enabled. This format is 1 sign bit, 12 integer bits, 8 filter bits and 11 fractional bits.

When MM8508_31 = 1, the format changes to S23.8.

Triangle DY Delta Register (TdDdY) (MMB524)

Read/Write Offset: B524H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DY DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DY DELTA HIGH															

Bits 31-0 DY DELTA

Value = Delta value for the accumulation of the D attribute with respect to Y. The format is S4.27.

Triangle VY Delta Register (TdVdY) (MMB528)

Read/Write Offset: B528H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VY DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VY DELTA HIGH															

Bits 31-0 VY DELTA

Value = Delta value for the accumulation of the V attribute with respect to Y. The format is S(4 + s).(27 - s) if perspective is enabled (3D command = 0101b or 0110b), where s is the number of mipmap levels programmed in MMB500_11-8. The format is S12.8.11 without perspective enabled. This format is 1 sign bit, 12 integer bits, 8 filter bits and 11 fractional bits.

When MM8508_31 = 1, the format changes to S23.8.

Triangle UY Delta Register (TdUdY) (MMB52C)

Read/Write Offset: B52CH (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UY DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
UY DELTA HIGH															

Bits 31-0 UY DELTA

Value = Delta value for the accumulation of the U attribute with respect to Y. The format is S(4 + s).(27 - s) if perspective is enabled (3D command = 0101b or 0110b), where s is the number of mipmap levels programmed in MMB500_11-8. The format is S12.8.11 without perspective enabled. This format is 1 sign bit, 12 integer bits, 8 filter bits and 11 fractional bits.

When MM8508_31 = 1, the format changes to S23.8.

Triangle D Start Register (TDS) (MMB530)

Read/Write Offset: B530H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D START															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	D START														

Bits 31-0 D START

Value = Starting value for the accumulation of the D attribute. The format is S4.27.

Triangle V Start Register (TVS) (MMB534)

Read/Write Offset: B534H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V START LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	V START HIGH														

Bits 31-0 V START

Value = Starting value for the accumulation of the V attribute. The format is S(4 + s).(27 - s) if perspective is enabled (3D command = 0101b or 0110b), where s is the number of mipmap levels programmed in MMB500_11-8. The format is S12.8.11 without perspective enabled. This format is 1 sign bit, 12 integer bits, 8 filter bits and 11 fractional bits. In either case, the sign bit must be 0.

The V attribute is the vertical coordinate value for a texel. When MM8508_31 = 1, the format changes to U23.8 with bit 31 = 0.

Triangle U Start Register (TUS) (MMB538)

Read/Write Offset: B538H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U START LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	U START HIGH														

Bits 31-0 U START

Value = Starting value for the accumulation of the U attribute. The format is S(4 + s).(27 - s) if perspective is enabled (3D command = 0101b or 0110b), where s is the number of mipmap levels programmed in MMB500_11-8. The format is S12.8.11 without perspective enabled. This format is 1 sign bit, 12 integer bits, 8 filter bits and 11 fractional bits. In either case, the sign bit must be 0.

The U attribute is the horizontal coordinate value for a texel. When MM8508_31 = 1, the format changes to U23.8 with bit 31 = 0.

Triangle GBX Delta Register (TdGdX_dBdX) (MMB53C)

Read/Write Offset: B53CH (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLUE X DELTA															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GREEN X DELTA															

Bits 15-0 BLUE X DELTA

Value = Delta value for the accumulation of the blue attribute with respect to X. The format is S8.7.

Bits 31-16 GREEN X DELTA

Value = Delta value for the accumulation of the green attribute with respect to X. The format is S8.7.

Triangle ARX Delta Register (TdAdX_dRdX) (MMB540)

Read/Write Offset: B540H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED X DELTA															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ALPHA X DELTA															

Bits 15-0 RED X DELTA

Value = Delta value for the accumulation of the red attribute with respect to X. The format is S8.7.

Bits 31-16 ALPHA X DELTA

Value = Delta value for the accumulation of the alpha attribute with respect to X. The format is S8.7.

Triangle GBY Delta Register (TdGdY_dBdY) (MMB544)

Read/Write Offset: B544H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLUE Y DELTA															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GREEN Y DELTA															

Bits 15-0 BLUE Y DELTA

Value = Delta value for the accumulation of the blue attribute with respect to Y. The format is S8.7.

Bits 31-16 GREEN Y DELTA

Value = Delta value for the accumulation of the green attribute with respect to Y. The format is S8.7.

Triangle ARY Delta Register (TdAdY_dRdY) (MMB548)

Read/Write Offset: B548H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED Y DELTA															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ALPHA Y DELTA															

Bits 15-0 RED Y DELTA

Value = Delta value for the accumulation of the red attribute with respect to Y. The format is S8.7.

Bits 31-16 ALPHA Y DELTA

Value = Delta value for the accumulation of the alpha attribute with respect to Y. The format is S8.7.

Triangle GB Start Register (TGS_BS) (MMB54C)

Read/Write Offset: B54CH (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	BLUE START														
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	GREEN START														

Bits 15-0 BLUE START

Value = Starting value for the accumulation of the blue attribute. The format is S8.7, where S must be 0.

Bits 31-16 GREEN START

Value = Starting value for the accumulation of the green attribute. The format is S8.7, where S must be 0.

Triangle AR Start Register (TAS_RS) (MMB550)

Read/Write Offset: B550H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RED START														
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	ALPHA START														

Bits 15-0 RED START

Value = Starting value for the accumulation of the red attribute. The format is S8.7, where S must be 0.

Bits 31-16 ALPHA START

Value = Starting value for the accumulation of the alpha attribute. The format is S8.7, where S must be 0.

Triangle ZX Delta Register (TdZdX) (MMB554)

Read/Write Offset: B554H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZX DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZX DELTA HIGH															

Bits 31-0 ZX DELTA

Value = Delta value for the accumulation of the Z attribute with respect to X. The format is S16.15.

Triangle ZY Delta Register (TdZdY) (MMB558)

Read/Write Offset: B558H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZY DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZY DELTA HIGH															

Bits 31-0 ZY DELTA

Value = Delta value for the accumulation of the Z attribute with respect to Y. The format is S16.15.

Triangle Z Start Register (TZS) (MMB55C)

Read/Write Offset: B55CH (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z START LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	Z START HIGH														

Bits 31-0 Z START

Value = Starting value for the accumulation of the Z attribute. The format is S16.15, where S must be 0.

The Z attribute is used in conjunction with z-buffering.

Triangle XY12 Delta Register (TdXdY12) (MMB560)

Read/Write Offset: B560H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XY12 DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XY12 DELTA HIGH															

Bits 31-0 XY12 DELTA

Value = Delta value for the accumulation of the X attribute with respect to Y along the 12 side. The format is S11.20.

See 3D Programming in Section 15 for an explanation of this field.

Triangle X12 End Register (TXEND12) (MMB564)

Read/Write Offset: B564H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X12 END LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	X12 END HIGH														

Bits 31-0 X12 END

Value = X coordinate for the last pixel drawn for side 12. The format is S11.20, where S must be 0.

See 3D Programming in Section 15 for an explanation of this field.

Triangle XY01 Delta Register (TdXdY01) (MMB568)

Read/Write Offset: B568H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XY01 DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XY01 DELTA HIGH															

Bits 31-0 XY01 DELTA

Value = Delta value for the accumulation of the X attribute with respect to Y along the 01 side. The format is S11.20.

See 3D Programming in Section 15 for an explanation of this field.

Triangle X01 End Register (TXEND01) (MMB56C)

Read/Write Offset: B56CH (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X01 END LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	X01 END HIGH														

Bits 31-0 X01 END

Value = X coordinate for the last pixel drawn for side 01. The format is S11.20, where S must be 0.

See 3D Programming in Section 15 for an explanation of this field.

Triangle XY02 Delta Register (TdXdY02) (MMB570)

Read/Write Offset: B570H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XY02 DELTA LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XY02 DELTA HIGH															

Bits 31-0 XY02 DELTA

Value = Delta value for the accumulation of the X attribute with respect to Y along the 02 side. The format is S11.20.

See 3D Programming in Section 15 for an explanation of this field.

Triangle X Start Register (TXS) (MMB574)

Read/Write Offset: B574H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X START LOW															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	X START HIGH														

Bits 31-0 X START

Value = Starting value for the accumulation of the X attribute. The format is S11.20, where S must be 0.

Triangle Y Start Register (TYS) (MMB578)

Read/Write Offset: B578H (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	Y START										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 Y START

Value = Starting value for the accumulation of the Y attribute.

Triangle Y Count Register (TY01_Y12) (MMB57C)

Read/Write Offset: B57CH (3D Triangle)
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SCAN LINE COUNT 12										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
L/R	R	R	R	R	SCAN LINE COUNT 01										

Bits 10-0 SCAN LINE COUNT 12

Value = The number of scan lines required to render the 12 side of the triangle.

See 3D Programming in Section 15 for a graphic description of this field. Either this field or the SCAN LINE COUNT 01 field below must be non-zero for the S3d Engine to draw a triangle.

Bits 15-11 Reserved

Bits 26-16 SCAN LINE COUNT 01

Value = The number of scan lines required to render the 01 side of the triangle.

See 3D Programming in Section 15 for a graphic description of this field. Either this field or the SCAN LINE COUNT 12 field above must be non-zero for the S3d Engine to draw a triangle.

Bits 30-27 Reserved

Bit 31 L/R - Left/Right Drawing Direction
0 = Render the triangle from right to left
1 = Render the triangle from left to right

The triangle must always be rendered in the direction starting with the triangle side with the largest Y component. See 3D Programming in Section 15 for a graphic description.

Section 20: Streams Processor Register Descriptions

Streams Processor registers can only be accessed via memory-mapped I/O. The register identifier MMxxxx means that this register is memory mapped at offset xxxx.

Color/Chroma Key Control (MM8184)

Read/Write Adds: 8184H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G/U/Cb KEY (LOW)								B/V/Cr KEY (LOW)							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KS	KMS		ST2	ST1	RGB CC			R/Y KEY (LOW)							

Bits 7-0 B/V/Cr key value (lower bound for chroma)

Bits 15-8 G/U/Cb key value (lower bound for chroma)

Bits 23-16 R/Y key value (lower bound for chroma)

Bits 26-24 RGB CC - RGB Color Comparison Precision
000 = Compare bit 7 of RGB (compare red bit 7's, green bit 7's and blue bit 7's)
001 = Compare bits 7-6 of RGB
010 = Compare bits 7-5 of RGB
011 = Compare bits 7-4 of RGB
100 = Compare bits 7-3 of RGB
101 = Compare bits 7-2 of RGB
110 = Compare bits 7-1 of RGB
111 = Compare bits 7-0 of RGB

Bit 27 ST1 - Streams Test Mode 1

This bit is for S3 use only and should never be programmed to 1.

Bit 28 ST2 - Streams Test Mode 2

This bit is for S3 use only and should never be programmed to 1.

Bits 30-29 KMS - Keying Mode Select
00 = Window keying (Opaque overlay of secondary stream over primary stream)
01 = Alpha keying (KRGB-16 1.5.5.5 or XRGB-32), with the K bit compared to bit 0 of this register or X bit compared to bits 7-0 of this register. Either the primary or secondary stream can be selected to generate the key depending on the setting of bit 31 of this register
10 = Color keying. Either the primary or secondary stream can be selected to generate the key depending on the setting of bit 31 of this register. For 8-bpp modes, color keying for the primary stream is generated using the 8-bit CLUT index, which is compared with bits 7-0 of 8184. Bits 23-8 must be all 0's. For 15- and 16-bpp modes, each color is padded to 8 bits by adding the appropriate number of 0's as lsbs.
11 = Chroma keying. The key can only be generated from the secondary stream, so bit 31 of this register must be set to 1.

Bit 31 KS - Key Select
0 = Select primary stream for keying
1 = Select secondary stream for keying

Secondary Stream Control (MM8190)

Read/Write Address: 8190H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DDA HORIZONTAL ACCUMULATOR											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	SFC			R	SDIF			HFD	R	R	R	R	R	R	R

Bits 11-0 DDA Horizontal Accumulator Initial Value

Value = 2 (W0-1) - (W1-1), where W0 is the line width in pixels before scaling and W1 is the line width in pixels after scaling. This is a signed value.

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 22-12 Reserved

Bit 23 HFD - Secondary Stream Horizontal Filtering Disable
0 = Secondary stream horizontal filtering not disabled when there is a secondary key match
1 = Secondary stream horizontal filtering disabled when there is a secondary key match

Bits 26-24 SDIF - Secondary Stream Input Data Format
000 = Reserved
001 = YCbCr-16 (4.2.2), 16-240 input range
010 = YUV-16 (4.2.2), 0-255 input range
011 = KRGB-16 (1.5.5.5)
100 = YUV (2.1.1)
101 = RGB-16 (5.6.5)
110 = RGB-24 (8.8.8)
111 = XRGB-32 (X.8.8.8)

When this field is programmed, the value does not take effect until the next VSYNC.

Bit 27 Reserved

Bits 30-28 SFC - Secondary Stream Horizontal Filter Characteristics
000 = Secondary stream
001 = Secondary stream, linear, 0-2-4-2-0, for X stretch
010 = Secondary stream, bi-linear, for 2X to 4X stretch
011 = Secondary stream, linear, 1-2-2-2-1, for 4X stretch
Other values reserved

When this field is programmed, the value does not take effect until the next VSYNC. Any valid setting can be used for any degree of stretch. The parenthetical comments are recommendations that may not be optimal in all cases.

Bit 31 Reserved

Chroma Key Upper Bound (MM8194)

Read/Write Address: 8194H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U/Cb KEY (UPPER)								V/Cr KEY (UPPER)							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	Y KEY (UPPER)							

Bits 7-0 V/Cr key value (upper bound)

Bits 15-8 U/Cb key value (upper bound)

Bits 23-16 Y key value (upper bound)

Bits 31-24 Reserved

Secondary Stream Stretch/Filter Constants (MM8198)

Read/Write Address: 8198H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	K1 HORIZONTAL SCALE FACTOR										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	K2 HORIZONTAL SCALE FACTOR										

Bits 10-0 K1 Horizontal Scale Factor

Value = W0-1, where W0 is the width in pixels of the initial output window (before scaling)

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 15-11 Reserved

Bits 26-16 K2 Horizontal Scale Factor

Value = W0-W1, where W0 is the initial (unscaled) window width in pixels and W1 is the final output window width in pixels. This is a signed value and will always be negative.

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-27 Reserved

Color Adjustment Register (MM819C)

Read/Write Offset: 819C
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCE	R	R	CONTRAST					BRIGHTNESS							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
HSE	R	R	HUE/SAT 2					R	R	R	HUE/SAT 1				

Bits 7-0 BRIGHTNESS - Brightness Control

Value = SBBBBBBB

where S is the sign bit (1 = negative) and BBBBBBB is the brightness adjustment factor. The larger the number, the greater the brightness. The value can range from -256 to 254 because the programmed value is shifted left by 1, thereby multiplying the value by 2. The value is in 2's complement format.

Bits 12-8 CONTRAST- Contrast Control

Value = C.CCCC

This is the contrast adjustment, which can vary from 0 to 1.9375. The value is in 2's complement format.

Bits 14-13 Reserved

Bits 15 BCE - Brightness and Contrast Enable
0 = Brightness and contrast control disabled
1 = Brightness and contrast control enabled

This control should be enabled only for YUV/YCbCr secondary stream formats and must be disabled for RGB secondary stream formats.

Bits 20-16 HUE/SAT 1 - Hue and Saturation Factor 1

Value = SF.FFF

where S is the sign bit (1 = negative) and F.FFF is the factor [SAT * cosine A]. SAT is the saturation, which can vary from -2 to 1.85 and A is the hue angle, the cosine of which can vary from -1 to +1. The value is in 2's complement format.

Bits 23-21 Reserved

Bits 28-24 HUE/SAT 2 - Hue and Saturation Factor 2

Value = SF.FFF

where S is the sign bit (1 = negative) and F.FFF is the factor [SAT * sine A]. SAT is the saturation, which can vary from -2 to 1.85 and A is the hue angle, the sine of which can vary from -1 to +1. The value is in 2's complement format.

Bits 30-29 Reserved

Bit 31 HSE - Hue and Saturation Control Enable
0 = Hue and saturation control disabled
1 = Hue and saturation control enabled

This control should be enabled only for YUV/YCbCr secondary stream formats and must be disabled for RGB secondary stream formats.

Blend Control (MM81A0)

Read/Write Address: 81A0H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	Kp				R	R	R	R	Ks				R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 1-0 Reserved

Bits 5-2 Ks

Value = secondary stream blend coefficient

The maximum value is 8. Kp + Ks must be ≤ 8. Blending is done according to the following formula; [Pp x Kp + Ps x Ks]/8. If Ks = 0, the result is a dissolve (see the definition for Kp below. If Ks is non-0, the result is a fade. When this field is programmed, the value does not take effect until the next VSYNC.

Bits 9-5 Reserved

Bits 13-10 Kp

Value = primary stream blend coefficient

The maximum value is 8. If Kp = 8, no blending is done. For a non-0 Kp and Ks = 0, the result is a fade according to the following formula: [Pp x Kp + Ps x (8 - Kp)]/8. When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-14 Reserved

Double Buffer/LPB Support (MM81CC)

Read/Write Address: 81CCH
Power-on Default: xxxxxx00H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	SBS	LST	LSL	LIS	ED	SBS		R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 Reserved

Bits 2-1 SBS - Secondary Stream Buffer Select
00 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream
01 = Secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream
10 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input stream. Which alternative applies is determined by LPB starting address register selected by bit 4 of this register
11 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input stream. Which alternative applies is determined by the LPB starting address register selected by bit 4 of this register

Bit 3 ED - Enable Deinterlacing
0 = Disable deinterlacing
1 = Enable deinterlacing

When deinterlacing is enabled, secondary stream vertical interpolation must be enabled, secondary stream vertical expansion must be set to 2x and double buffering must be enabled. Secondary stream buffer 0 is assumed to contain the odd field and buffer 1 is assumed to contain the even field. Bit 7 of this register must be set to 1 when this function is enabled. Note that de-interlacing can be done more generally using the two DDA's defined in MM81E8H, so normally this bit should never be set.

Bit 4 LIS - LPB Input Buffer Select
0 = LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input
1 = LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input

This bit selects the starting address for writing LPB data into the frame buffer. When the value programmed to this bit takes effect is determined by the setting of bit 5 of this register. This bit can be toggled at the completion of writing all the data for a frame to the frame buffer via bit 6 of this register

Bit 5 LSL - LPB Input Buffer Select Loading
0 = The value programmed into bit 4 of this register takes effect immediately
1 = The value programmed into bit 4 of this register takes effect at the next end of frame (completion of writing all the data for a frame into the frame buffer)

Bit 6 LST - LPB Input Buffer Select Toggle
0 = End of frame (completion of writing all the data for a frame into the frame buffer) has no effect on the setting of bit 4 of this register
1 = End of frame causes the setting of bit 4 of this register to toggle

Bit 7 SBS - Secondary Buffer Address Control
0 = No effect
1 = Secondary buffer address synchronized

This bit must be set to 1 when bit 3 of this register is set to 1. It will normally be left at 0.

Bits 31-7 Reserved

Secondary Stream Frame Buffer Address 0 (MM81D0)

Read/Write Address: 81D0H
Power-on Default: Undefined

If a secondary stream is enabled, this register specifies the starting address in the frame buffer

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECONDARY BUFFER ADDRESS 0															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	SECONDARY BUFFER ADDRESS 0					

Bits 21-0 Value = Secondary stream frame buffer starting address 0

This value must be quadword aligned.

Bits 31-22 Reserved

Secondary Stream Frame Buffer Address 1 (MM81D4)

Read/Write Address: 81D4H
Power-on Default: Undefined

If the secondary stream is double buffered, this register specifies the starting address in the frame buffer for the second buffer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECONDARY BUFFER ADDRESS 1															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	SECONDARY BUFFER ADDRESS 1					

Bits 21-0 Value = Secondary stream frame buffer starting address 1

This value must be quadword aligned.

Bits 31-22 Reserved

Secondary Stream Stride (MM81D8)

Read/Write Address: 81D8H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	SECONDARY STREAM STRIDE											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 11-0 Secondary stream stride

Value = byte offset of vertically adjacent pixels in the secondary stream buffer(s)

If double buffering is used, the stride must be the same for both buffers. The low order 4 bits of this value must be 0000b.

Bits 31-12 Reserved

Opaque Overlay Control (MM81DC)

Read/Write Address: 81DCH
Power-on Default: Undefined except bits 31-30 are 00b.

When an opaque overlay is being used (bit 31 of this register = 1), the fields in this register can be programmed to eliminate the fetching of the pixels for the rectangular area under the top (opaque) window (secondary stream). This reduces the memory bandwidth requirements. None of the fields in this register have an effect unless bit 31 is set to 1. Note that only horizontal coordinates must be specified. The vertical coordinates are handled automatically by the hardware.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	PIXEL STOP FETCH										R	R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OOC	R=0	R	PIXEL RESUME FETCH										R	R	R

Bits 2-0 Reserved

Bits 12-3 Pixel Stop Fetch

Value = [Offset in 16-byte units from the background starting pixel horizontal position to the first pixel of the line not to be fetched from memory (hidden background)] + 1 16-byte unit

MM81F8_26-16 define the first pixel position for each line in the top window (X1). The latter is the first background pixel that does not need to be fetched. The value programmed in this field is then [X1 x bytes per pixel/16] +1. If the result is a fraction, it is rounded up the next highest integer. This gives the required quadword offset (O) for this field. This value is also used in the calculation for the field value of bits 28-19 of this register.

Bits 18-13 Reserved

Bits 28-19 Pixel Resume Fetch

Value = {Offset in 16-byte units from the background starting pixel horizontal position to the line position of the resumption of pixel fetching from memory (i.e., visible background)} - 1 16-byte unit

The value is determined by adding the Pixel Stop Fetch field value (O) above (bits 12-3) to the width in 16-byte units of the top (secondary stream) window (W). The width of the top window in pixels (P) is found in MM81FC_26-16. W in 16-byte units = P x bytes per pixel/16. If this is a fraction, the result is truncated to the next lowest integer. The value in this field is then [W + O] - 1.

Bit 29 Reserved

Bit 30 Reserved = 0

This bit must never be set to 1.

Bit 31 OOC - Opaque Overlay Control Enable
0 = Opaque overlay control disabled
1 = Opaque overlay control enabled

K1 Vertical Scale Factor (MM81E0)

Read/Write Address: 81E0H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	K1 VERTICAL SCALE FACTOR										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 K1 Vertical Scale Factor

Value = [height (in lines) of the initial output window (before scaling)] - 1

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-11 Reserved

K2 Vertical Scale Factor (MM81E4)

Read/Write Address: 81E4H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	K2 VERTICAL SCALE FACTOR										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 K2 Vertical Scale Factor

Value = [height (in lines) of the initial output window (before scaling)] - [height (in lines) of the final output window (after scaling)]

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-11 Reserved

DDA Vertical Accumulator Initial Value (MM81E8)

Read/Write Address: 81E8H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSVI	BS	R	R	DDA VERTICAL ACCUMULATOR 0											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	DS	DDA VERTICAL ACCUMULATOR 1											

Bits 11-0 DDA Vertical Accumulator Initial Value 0

Value = 2's complement of {[height (in lines) of the output window after scaling] - 1}

This value is used when bit 28 of this register is set to 0. If bit 28 is set to 1 this value is used only when the secondary stream comes from secondary buffer 0. When this field is programmed, the value does not take effect until the next VSYNC.

Bit 13-12 Reserved

Bit 14 BS - Enable Bandwidth Savings Mode
0 = Normal operation
1 = Enable bandwidth savings mode (secondary stream interpolation)

Bit 15 SSVI - Enable Secondary Stream Vertical Interpolation
0 = Secondary stream vertical interpolation disabled
1 = Secondary stream vertical interpolation enabled

Secondary stream vertical interpolation must be disabled when 3-line flicker filtering is enabled (SR70_0 = 1 and SR70_1 = 0).

Bits 27-16 DDA Vertical Accumulator Initial Value 1

Value = 2's complement of {[height (in lines) of the output window after scaling] - 1}

This value is used when bit 28 of this register is set to 1 and the secondary stream comes from secondary buffer 1. When this field is programmed, the value does not take effect until the next VSYNC.

Bit 28 DS - DDA Vertical Accumulator Initial Value Select
0 = Use only DDA Vertical Accumulator Initial Value 0
1 = Use both DDA Vertical Accumulator Initial Value 0 and 1

This setting should only be used with double buffering and an interlaced video source.

Bits 31-29 Reserved

Secondary Window Start Coordinates (MM81F8)

Read/Write Address: 81F8H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SECONDARY STREAM Y-START										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	SECONDARY STREAM X-START										

Bits 10-0 Secondary Stream Y-Start

Value = Screen line number +1 of the first line of the secondary stream window

Bits 15-11 Reserved

Bits 26-16 Secondary Stream X-Start

Value = Screen pixel number +1 of the first pixel of the secondary stream window

Bits 31-27 Reserved

Secondary Window Size (MM81FC)

Read/Write Address: 81FCH
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SECONDARY STREAM HEIGHT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	SECONDARY STREAM WIDTH										

Bits 10-0 Secondary Stream Height

Value = Number of lines displayed in the secondary stream window

Bits 15-11 Reserved

Bits 26-16 Secondary Stream Width

Value = Number of pixels -1 displayed in each line in the primary stream window

Bits 31-27 Reserved

Section 21: DMA Register Descriptions

This section describes the Direct Memory Access (DMA) registers for M5. These registers are used to control the two DMA channels when M5 operates as a PCI bus master. The video/graphics data transfer channel handles:

- Compressed video data transfers from system memory to an MPEG-1 decoder via the LPB
- Decompressed video data (software MPEG) transfers to the frame buffer via the LPB
- Frame buffer data transfers to system memory

For the latter case, the video memory read data location and structure are specified in MM8220 and MM8224.

The command data channel handles transfers of command and drawing parameter data from system memory to the S3D Engine.

These two channels can operate independently.

In all register bit descriptions, the letter "R" identifies reserved bits (a reserved bit's read value is undefined unless noted, and you may write only zero to a reserved bit).

21.1 DMA READ REGISTERS

DMA Read Base Address Register (MM8220)

Read/Write Offset: 8220H
Power-On Default: Undefined

This register is used when the CPU is doing DMA transfers from video memory as specified by clearing bit 1 of MM8580 to 0 (read) and setting bit 0 of MM8588 to 1 (video DMA enable).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA READ BASE ADDRESS													0	0	0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	DMA READ BASE ADDRESS						

Bits 2-0 Reserved = 0

Bits 22-3 DMA READ BASE ADDRESS

Value = Starting address in video memory for data to be DMAed to system memory (quadword aligned)

Bits 31-23 Reserved

DMA Read Stride/Width Register (MM8224)

Read/Write Offset: 8224H
Power-On Default: Undefined

This register is used when the CPU is doing DMA transfers from video memory as specified by clearing bit 1 of MM8580 to 0 (read) and setting bit 0 of MM8480 to 1 (video DMA enable).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DMA READ STRIDE									0	ATC	
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	DMA READ WIDTH									0	0	0

Bits 1-0 ATC - Address Tiling Control
00 = CPU address lines 14-8 are sequential (linear addressing)
01 = CPU address lines 14-8 are rearranged to 14, 9, 8, 13, 12, 11, 10
10 = CPU address lines 14-8 are rearranged to 10, 9, 8, 14, 13, 12, 11
11 = CPU address lines 14-8 are sequential (linear addressing)

The rearranged settings provide a narrower and deeper memory page size to minimize page breaks when drawing is limited to a small area of the screen. The 10 setting provides the narrowest page size.

Bit 2 Reserved = 0

Bits 11-3 DMA READ STRIDE

Value = Number of quadwords to add to the address at the end of a line to generate the address for the next line to be transferred

A DMA transfer from video memory to system memory starts at the address specified in MM8220_22_3 and proceeds for the number of quadwords defined by the value in bits 27-19 of this register. The stride value is then added to end of line address to get the address for the start of the next line to be transferred.

Bits 15-12 Reserved

Bits 18-16 Reserved = 0

Bits 27-19 DMA READ WIDTH

Value = [Number of quadwords per line to transfer to system memory] - 1

Bits 31-28 Reserved

21.2 VIDEO/GRAPHICS DATA TRANSFER CHANNEL

Video DMA Starting System Memory Address Register (MM8580)

Read/Write Offset: 8580H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STARTING MEMORY ADDRESS														R/W	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
STARTING MEMORY ADDRESS															

Bit 0 Reserved

Bit 1 R/W - Video/Graphics DMA Read/Write
0 = Video DMA write (system memory to the LPB output FIFO)
1 = Video DMA read (video memory to system memory)

Data written to the LPB output FIFO can be directed to an MPEG decoder (compressed data) or to video memory with optional decimation.

Bits 31-2 STARTING MEMORY ADDRESS

Value = Starting memory address when performing a DMA transfer from video memory to system memory or from system memory to the LPB output FIFO

Video DMA Transfer Length Register (MM8584)

Read/Write Offset: 8584H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA TRANSFER LENGTH														R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	DMA TRANSFER LENGTH							

Bits 1-0 Reserved

Bits 23-2 DMA TRANSFER LENGTH

Value = (Number of double words to transfer) - 1.

Bits 31-24 Reserved

Video DMA Transfer Enable Register (MM8588)

Read/Write Offset: 8588H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	VDE
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 VDE - Video/Graphics DMA Enable
0 = Disable video/graphics DMA
1 = Enable video graphics DMA

This bit is reset to 0 by the DMA controller at the completion of a video/graphics DMA transfer.

Bits 31-1 Reserved

21.3 COMMAND TRANSFER CHANNEL

Command DMA Base Address Register (MM8590)

Read/Write Offset: 8590H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE ADDRESS				R	R	R	R	R	R	R	R	R	R	BS	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASE ADDRESS															

Bit 0 Reserved

Bit 1 BS - Command DMA Buffer Size
0 = 4 KByte buffer size
1 = 64 KByte buffer size

Bits 11-2 Reserved

Bits 31-12 BASE ADDRESS

Value = Command DMA buffer base address

Bits 15-12 must be 000b for a 64K buffer size (64K aligned).

Command DMA Write Pointer Register (MM8594)

Read/Write Offset: 8594H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRITE POINTER														R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	WPU

Bits 1-0 Reserved

Bits 15-2 WRITE POINTER

Value = next doubleword address after the last doubleword written to the system memory buffer

Software should verify that the write pointer value equals the read pointer value before disabling DMA operation.

Bit 16 WPU - Write Pointer Updated

Software must set this bit to 1 each time it updates the write pointer.

Bits 31-17 Reserved

Command DMA Read Pointer Register (MM8598)

Read/Write Offset: 8598H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ POINTER														R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 1-0 Reserved

Bits 15-2 READ POINTER

Value = Address of next doubleword in system memory to be read by the DMA

4K buffer: address = base address 31-12 (concat) read pointer 11-2 (concat) 00
64K buffer: address = base address 31-16 (concat) read pointer 15-2 (concat) 00

After this pointer value is initialized, it is is updated automatically by ViRGE.

Bits 31-16 Reserved

Command DMA Enable Register (MM859C)

Read/Write Offset: 859CH
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	CDE
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 CDE - Command DMA Enable
0 = Command DMA Disabled
1 = Command DMA Enabled

Bits 31-1 Reserved

Section 22: Miscellaneous Register Descriptions

In all register bit descriptions, the letter "R" identifies reserved bits (a reserved bit's read value is undefined unless noted, and you may write only zero to a reserved bit).

Subsystem Status Register (MM8504)

Read Only Offset: 8504H
Power-On Default: Undefined

This read-only register provides information on interrupt status, monitor I.D. and the number of bits per pixel. See the Subsystem Control (MM8504, Write Only) register for details on enabling and clearing interrupts.

15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
S3d FIFO 6-5		S3d ENG	S3d FIFO SLOTS FREE (4-0)					LPB INT	3DF FIFO	CD DON	HD DON	FIFO EMP	FIFO OVF	3D DON	C1 VI
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	C2VI

Bit 0 C1 VI - Controller 1 Vertical Sync Interrupt Status
0 = No interrupt
1 = Interrupt generated

Bit 1 3D DON - S3d Engine Done Interrupt Status
0 = No interrupt
1 = Interrupt generated

Bit 2 FIFO OVF - Command FIFO Overflow Interrupt Status
0 = No interrupt
1 = Interrupt generated

Bit 3 FIFO EMP - Command FIFO Empty Interrupt Status
0 = No interrupt
1 = Interrupt generated

Bit 4 HD DON - Host DMA Done Interrupt Status
0 = No interrupt
1 = Interrupt generated

Bit 5 CD DON - Command DMA Done Interrupt Status
0 = No interrupt
1 = Interrupt generated

Bit 6 3DF FIF - S3d FIFO Empty Status
0 = No interrupt
1 = Interrupt generated

Bit 7 LPB INT - LPB Interrupt Status
0 = No interrupt
1 = Interrupt generated

LPB interrupts are enabled and cleared via MMFF08. Any LPB interrupt will set this bit.

Bits 12-8 S3d FIFO SLOTS FREE Bits 4-0

Value = # of S3d FIFO slots empty

Bits 6-5 of this value are bit 15-14 of this register. However, bit 12 is the OR of bits 12, 14 and 15. Software should use either bits 12-8 (backward compatible) or bits 15-14 (16-bit increments).

Bit 13 S3d ENG - S3d Engine Status
0 = S3d Engine busy
1 = S3d Engine idle

Bits 15-14 S3d FIFO SLOTS FREE Bits 6-5

See bits 12-8 of this register. These are the 2 msb's of the FIFO slots free status.

Bit 16 C2 VI - Controller 2 Vertical Sync Interrupt Status
0 = No interrupt
1 = Interrupt generated

Bits 31–17 Reserved

Subsystem Control Register (MM8504)

Write Only Offset: 8504H
Power-On Default: Undefined

This register allows each of several interrupt sources to be enabled or disabled. Interrupt status (Subsystem Status (MM8504, Read Only) can be cleared. This register also controls the software reset of the graphics engine.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S3d RST 1	0	3DF ENB	CDD ENB	FIFO EMP	ENB OVF	3DD ENB	VSY ENB	HDD ENB	3DF CLR	CDD CLR	HDD CLR	FIFO CLE	FIFO CLO	3DD CLR	C1VI CLR
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	C2VI	R

Bit 0 C1VI CLR - Clear Controller 1 Vertical Sync Interrupt Status
0 = No change
1 = Clear

Bit 1 3DD CLR - Clear S3d Engine Done Interrupt Status
0 = No change
1 = Clear

Bit 2 FIFO CLO - Clear Command FIFO Overflow Interrupt Status
0 = No change
1 = Clear

Bit 3 FIFO CLE - Clear Command FIFO Empty Interrupt Status
0 = No change
1 = Clear

Bit 4 HDD CLR - Clear Host DMA Done Interrupt Status
0 = No change
1 = Clear

Bit 5 CDD CLR - Clear Command DMA Done Interrupt Status
0 = No change
1 = Clear

Bit 6 3DF CLR - Clear S3d FIFO Empty Interrupt Status
0 = No change
1 = Clear

Bit 7 HDD ENB - Host DMA Done Interrupt Enable
0 = Disable
1 = Enable interrupt when a host DMA transfer is complete and CR32_4 = 1

Bit 8 C1VI ENB - Controller 1 Vertical Sync Interrupt Enable
0 = Disable
1 = Enable interrupt when VSYNC goes active and CR32_4 = 1

Bit 9 3DD ENB- S3d Engine Done Interrupt Enable
0 = Disable
1 = Enable interrupt when the S3d Engine completes its current task and becomes idle and CR32_4 = 1

Bit 10 FIFO ENB OVF - Command FIFO Overflow Interrupt Enable
0 = Disable
1 = Enable interrupt when the command FIFO overflows and CR32_4 = 1

Bit 11 FIFO ENB EMP - Command FIFO Empty Interrupt Enable
0 = Disable
1 = Enable interrupt when the command FIFO becomes empty and CR32_4 = 1

Bit 12 CDD ENB - Command DMA Done Interrupt Enable
0 = Disable
1 = Enable interrupt when a command DMA transfer is complete and CR32_4 = 1

Bit 13 3DF ENB - S3d FIFO Empty Interrupt Enable
0 = Disable
1 = Enable interrupt when the S3d FIFO becomes empty and CR32_4 = 1

Bits 15–14 S3d RST - S3d Engine Software Reset
00 = No change
01 = S3d Engine enabled
10 = Reset
11 = Reserved

Setting CR66_1 to 1 is equivalent to setting these bits to 10b.

Bit 16 Reserved

Bit 17 C2VI - Controller 2 Vertical Sync Interrupt Enable
0 = Disable
1 = Enable interrupt when VSYNC goes active and CR32_4 = 1

Bits 31-18 Reserved

Advanced Function Control Register (MM850C)

See Bit Descriptions Offset: 850CH
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	CMD FIFO STATUS					R	LA ENB	R	R	RST DM	ENB EHFC
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 ENB EHFC - Enable Enhanced Functions (Read/Write)
0 = Enable VGA and VESA planar (4 bits/pixel) modes
1 = Enable all other modes (Enhanced and VESA non-planar)

This bit is ORed with bit 0 of CR66 and is equivalent to it.

Bit 1 RST DM - Reset Read DMA (Read/Write)
0 = No effect
1 = Reset read DMA pointers

This bit should be toggled (program a 1 and then a 0) by software immediately after the completion of each read DMA operation.

Bits 3-2 Reserved

Bit 4 LA ENB- Linear Addressing Enable
0 = Disable linear addressing
1 = Enable linear addressing

This bit is ORed with bit 4 of CR58 and is equivalent to it.

Bit 5 Reserved

Bits 10-6 COMMAND FIFO STATUS (Read Only)

Value = Number of Command FIFO slots free

For example, a value of 00101 indicates 5 slots are free. This is a 16-slot FIFO.

Bits 31–11 Reserved

Section 23: Local Peripheral Bus Register Descriptions

LPB registers can only be accessed via memory-mapped I/O. The register identifier MMxxxx means that the register is memory mapped at offset xxxx from the base address.

LPB Mode (MMFF00)

See Bit Descriptions Address: FF00H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LBA	CHS	CVS	LHS	LVS	R	HDM	CBS	SF	LR	LPB MODE			LE
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BAS		IOD	O/E	R	ILC	SNO	CS	R	R	R	EHD	VSH	R	MBS	

Bit 0 LE - LPB Enable
0 = LPB Disabled
1 = LPB Enabled

Once enabled, the LPB is reset either by a system reset or via bit 4 of this register.

Bits 3-1 LPB MODE
000 = Bidirectional Mode
001 = Video 16 Mode. This mode is also used for ZV Port operation.
010 = Video 8 In Mode
100 = Pass-through Mode. 32-bit data from the output FIFO is passed directly to the decimation input to the video FIFO. This allows decimation of CPU-provided data.

All other values are reserved.

Bit 4 LR- LPB Reset
0 = No effect
1 = Reset LPB

This bit should be set and then reset before switching between LPB modes.

Bit 5 SF - Skip Frames
0 = Write all received frames to memory
1 = Write every other received frame to memory (1, 3, etc.)

Bit 6 CBS - Color Byte Swap
0 = Incoming video is in U_{01}, Y_0, V_{01}, Y_1 format, byte swap enabled
1 = Incoming video is in Y_0, U_{01}, Y_1, V_{01} format (e.g., SAA7110), no byte swap

This function only applies to Video 8 mode with bit 7 of this register = 1.

Bit 7 HDM - Horizontal Decimation Mode
0 = Decimation uses method described in MMFF2C
1 = Decimation uses method described in Section 12-5

Bit 8 Reserved

Bit 9 LVS - LPB Vertical Sync Input Polarity
0 = LPB vertical sync input is active low
1 = LPB vertical sync input is active high

Bit 10 LHS - LPB Horizontal Sync Input Polarity
0 = LPB horizontal sync input is active low
1 = LPB horizontal sync input is active high

Bit 11 CVS - CPU VSYNC (Write Only)

Writing a 1 to this bit causes the M5 to do whatever functions it is programmed to do upon receipt of a VSYNC. For example, values programmed in certain registers only take effect at the next VSYNC.

Bit 12 CHS - CPU HSYNC (Write Only)

Writing a 1 to this bit causes the M5 to do whatever functions it is programmed to do upon receipt of an HSYNC.

Bit 13 LBA - Load Base Address (Write Only)

Writing a 1 to this bit immediately loads the base address currently being pointed to.

Bit 15-14 Reserved

Bits 17-16 MBS - Maximum LPB to Scenic/MX2 Compressed Data Burst Size (Bidirectional mode only)
00 = Burst 1 32-bit word
01 = Burst 2 32-bit words
10 = Burst 3 32-bit words
11 = Burst all 32-bit words (until empty)

With a setting of 11b, software must ensure that no more than eight 32-bit words are burst to the Scenic/MX2 in a single burst. For example, if the FIFO is full (8 entries), no more entries should be written until the burst is complete.

Bit 18 Reserved

Bit 19 VSH - Data Capture When VS is High
0 = Normal operation (no data captured when VS is high)
1 = Capture data when VS is high

This function applies to Video 8 and Video 16 modes and is usually used to capture VBI data.

Bit 20 EHS - Early HREF Detection
0 = Normal operation (no early HREF detection)
1 = Flush video FIFO if HREF occurs before widow width is reached

This function applies to Video 8 and Video 16 modes and is usually used to capture VBI data.

Bits 23-21 Reserved

Bit 24 CS - LPB Clock Source
0 = LPB clock driven by SCLK
1 = LPB clock driven by LCLK

LCLK is used when an external peripheral is connected to the LPB. SCLK is used for pass-through mode.

Bit 25 SNO - Sync Non-Overlap
0 = No effect
1 = Don't add stride after first HSYNC

This bit must be set when the first HSYNC does not occur within the VSYNC active period.

Bit 26 ILC - Invert LCLK
0 = Use LCLK as received
1 = Invert the LCLK input

Bit 27 BAS - Base Address Select Status (Read Only)
0 = LPB base address 0 selected
1 = LPB base address 1 selected

Bit 28 O/E - Odd/Even Frame Status (Read Only)
0 = Odd frame being written to frame buffer
1 = Even frame being written to frame buffer

This bit will normally be used for frame capture. If the ODD pin function is enabled and ZV-Port operation is not enabled, this bit reports the status of the ODD pin (0 = odd field, 1 = even field). If ZV-Port operation is enabled, this bit reports the status of the automatic odd/even field detection based on VS and HREF.

Bit 29 IOD - Invert Odd/Even Frame Indicator
0 = Odd/Even frame indicator unchanged
1 = Odd/Even frame indicator inverted

This inverts the odd/even frame indicator (bit 28).

Bit 30 IE - Interlace Enable
0 = Interlacing disabled
1 = Interlacing enabled

Bit 31 ZVP - ZV Port Enable
0 = ZV Port disabled. Use ODD pin status when interlacing is enabled.
1 = ZV Port operation enabled (automatic detection of odd/even fields when interlacing is enabled.

LPB FIFO Status (MMFF04)

Read Only Address: FF04H
Power-on Default: 00000008H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	OFAE	OFE	OFF	R	R	R	R	R	R	R	OFIFO STATUS			
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VF1AE	VF1E	VF1F	R	R	R	R	R	R	VF0AE	BST	VFF	R	R	R	R

Bits 3-0 LPB Output FIFO Status
0000 = 0 FIFO slots free
0001 = 1 FIFO slot free
0010 = 2 FIFO slots free
0011 = 3 FIFO slots free
0100 = 4 FIFO slots free
0101 = 5 FIFO slots free
0110 = 6 FIFO slots free
0111 = 7 FIFO slots free
1000 = 8 FIFO slots free

Each slot contains 4 bytes

Bits 10-4 Reserved

Bit 11 OFF - LPB Output FIFO Full
0 = Output FIFO not full
1 = Output FIFO full

Bit 12 OFE - LPB Output FIFO Empty
0 = Output FIFO not empty
1 = Output FIFO empty

Bit 13 OFAE - LPB Output FIFO Almost Empty
0 = Output FIFO has something other than 1 slot filled
1 = Output FIFO has one slot filled

Bits 19-14 Reserved

Bit 20 VFF - LPB Video FIFO Full
0 = Video FIFO is not full
1 = Video FIFO full

Bit 21 VFE - LPB Video FIFO Empty
0 = Video FIFO not empty
1 = Video FIFO empty

Bit 22 VFAE - LPB Video FIFO Almost Empty
0 = Video FIFO has something other than 1 slot filled
1 = Video FIFO has one slot filled

Bits 31-23 Reserved

LPB Interrupt Flags (MMFF08)

Read/Write Address: FF08H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	VTE	R	R	R	SPS	EFI	ELI	FEI
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	SPW	VTM	R	R	R	SPM	EFM	ELM	FEM

Bit 0 FEI - LPB Output FIFO Empty Interrupt Status
0 = No interrupt
1 = LPB output FIFO empty

Writing a 1 to this bit clears the interrupt.

Bit 1 ELI - End of Line Interrupt Status
0 = No interrupt
1 = HSYNC input received

Writing a 1 to this bit clears the interrupt.

Bit 2 EFI - End of Frame Interrupt Status
0 = No interrupt
1 = VSYNC input (leading edge of VSYNC) received

Writing a 1 to this bit clears the interrupt.

Bit 3 SPS - Serial Port Start Detect Interrupt Status
0 - No interrupt
1 = Serial port start condition detected

A serial port start condition occurs when the SPDAT pin is driven low by another device while the SPCLK pin is not being driven low. Writing a 1 to this bit clears the interrupt.

Bits 6-4 Reserved

Bit 7 VTE - VSYNC Trailing Edge Interrupt Status
0 = No interrupt
1 = VSYNC trailing edge input received

Bits 15-8 Reserved

Bit 16 FEM - LPB Output FIFO Empty Interrupt Enable Mask
0 = LPB output FIFO empty interrupt disabled
1 = LPB output FIFO empty interrupt enabled

Bit 17 ELM - End of Line Interrupt Enable Mask
0 = End of Line interrupt disabled
1 = End of Line interrupt enabled

Bit 18 EFM - End of Frame Interrupt Enable Mask
0 = End of frame interrupt disabled
1 = End of frame interrupt enabled

Bit 19 SPM - Serial Port Start Detect Interrupt Mask
0 = Serial port start detect interrupt disabled
1 = Serial port start detect interrupt enabled

Bits 22-20 Reserved

Bit 23 VTM - VSYNC Trailing Edge Interrupt Enable Mask
0 = VSYNC trailing edge interrupt disabled
1 = VSYNC trailing edge interrupt enabled

Bit 24 SPW - Serial Port Wait
0 = Release SPCLK to float high
1 = Drive SPCLK low upon receipt of a serial port start condition

Setting this bit to 1 enables serial port wait states until the host is ready to process the data.

Bit 31-25 Reserved

LPB Frame Buffer Address 0 (MMFF0C)

Read/Write Address: FF0CH
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB BUFFER ADDRESS 0														R=0	R=0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	LPB BUFFER ADDRESS 0					

Bits 21-0 LPB Frame Buffer Address 0

Value = starting address 0 (offset in bytes from the start of the frame buffer) for writing LPB data to the frame buffer

This value will normally be the same as the secondary stream frame buffer address 0. The value must start on an 8-byte boundary. The two low order bits are force to 0. A value programmed in this field does not take effect until the next LPB VSYNC.

Bits 31-22 Reserved

LPB Frame Buffer Address 1 (MMFF10)

Read/Write Address: FF10H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB BUFFER ADDRESS 1														R=0	R=0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	LPB BUFFER ADDRESS 1					

Bits 21-0 LPB Frame Buffer Address 1

Value = starting address 1 (offset in bytes from the start of the frame buffer) for writing LPB data to the frame buffer

This value will normally be the same as the secondary stream frame buffer address 1. Both address 0 and address 1 are defined when double buffering is used. The value must start on an 8-byte boundary. The two low order bits are forced to 0. A value programmed in this field does not take effect until the next LPB VSYNC.

Bits 31-22 Reserved

LPB Direct Read/Write Address (MMFF14)

Read/Write Address: FF14H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB DIRECT READ/WRITE ADDRESS															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R					

Bits 20-0 LPB Direct Read/Write Address

Value = address of video decoder register to read/write

Bits 31-21 Reserved

LPB Direct Read/Write Data (MMFF18)

Read/Write Address: FF18H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB DIRECT READ/WRITE DATA															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LPB DIRECT READ/WRITE DATA															

Bits 31-0 LPB Direct Read/Write Data

A write to this register triggers a read/write sequence based on the address information in MMFF14_23-0.

LPB General Purpose Input/Output Port (MMFF1C)

Read/Write - see bit definitions Address: FF1CH
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	LPB GIP				LPB GOP			
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 3-0 LPB General Purpose Output Data Port

These bits are driven onto the LPB LD[3:0] lines whenever a write is performed to CR5C. STWR is asserted (low) at this time for use as an enable strobe for latching the data into an external buffer.

Bits 7-4 LPB General Purpose Input Data Port (Read only)

Whenever a write is performed to CR5C, STWR is asserted (low). This strobe can be used to enable a register to drive data onto any or all of the LD[7:4] lines. This data is then latched into these bits.

Bits 31-8 Reserved

Serial Port (MMFF20)

Read/Write Address: FF20H
Power-on Default: 00000000H

This register can also be accessed at I/O ports E2H or E8H. See the Serial Communications Port description in Section 4.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	B4M	B3M	B2M	B1M	B0M	R	R	R	SPE	SDR	SCR	SDW	SCW
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 SCW - Serial Clock Write
0 = SPCLK pin is driven low
1 = SPCLK pin is tri-stated

The SPCLK pin carries the DDC/I^2C clock, depending on the operational mode. When it is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 2 of this register.

Bit 1 SDW - Serial Data Write
0 = SPDAT pin is driven low
1 = SPDAT pin is tri-stated

The SPDAT pin carries the DDC/I^2C data, depending on the operational mode. When it is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 3 of this register.

Bit 2 SCR - Serial Clock Read (Read Only)
0 = SPCLK pin is low
1 = SPCLK pin is tri-stated (no device is driving this line)

Bit 3 SDR - Serial Data Read (Read Only)
0 = SPDAT pin is low
1 = SPDAT pin is tri-stated (no device is driving this line)

Bit 4 SPE - Serial Port Enable
0 = Use of bits 1-0 of this register disabled
1 = Use of bits 1-0 of this register enabled

Bits 5-7 Reserved

Bit 8 B0M - Bit 0 Mirror (Read Only)
0 = SPCLK pin is driven low
1 = SPCLK pin is tri-stated

Bit 9 B1M - Bit 1 Mirror (Read Only)
0 = SPDAT pin is driven low
1 = SPDAT pin is tri-stated

Bit 10 B2M - Bit 2 Mirror (Read Only)
0 = SPCLK pin is low
1 = SPCLK pin is tri-stated (no device is driving this line)

Bit 11 B3M -Bit 3 Mirror (Read Only)
0 = SPDAT pin is low
1 = SPDAT pin is tri-stated (no device is driving this line)

Bit 12 B4M - Bit 4 Mirror (Read Only)
0 = Use of bits 1-0 of this register disabled
1 = Use of bits 1-0 of this register enabled

This bit mirrors bit 4 and allows reading of this data on byte lane 2 at I/O address E2H.

Bits 31-13 Reserved

LPB Video Input Window Size (MMFF24)

Read/Write Address: FF24H
Power-on Default: Undefined

This register applies only to Video 8 In or Video 16 mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	VIDEO INPUT LINE WIDTH											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	VIDEO INPUT WINDOW HEIGHT								

Bits 11-0 Video Input Line Width

Value = [# pixels x 2] - 2 for Video 8 mode
Value = # pixels -2 for Video 16 mode

This is the width of the displayed line after the offset specified in MMFF28_11-0. Before the 2 is subtracted, the number of pixels must be a multiple of 8. For example, in Video 16 mode, if the line width is 637 pixels, this must be rounded up to 640. The programmed value is then 640 - 2 = 638.

Bits 15-12 Reserved

Bits 24-16 Video Input Window Height

Value = [height in lines of each video input frame] - 1

This is the number of displayed lines - 1 after the offset specified in MMFF28_24_16.

Bits 31-25 Reserved

LPB Video Data Offsets (MMFF28)

Read/Write Address: FF28H
Power-on Default: Undefined

This register applies only to Video 8 In or Video 16 mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	HORIZONTAL VIDEO DATA OFFSET											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	VERTICAL VIDEO DATA OFFSET								

Bits 11-0 Horizontal Video Data Offset

Value = [number of LCLKs between HSYNC and the start of valid pixel data] - 2

Bits 15-12 Reserved

Bits 24-16 Vertical Video Data Offset

Value = number of HSYNCs between VSYNC and the first valid data line

Bits 31-25 Reserved

LPB Horizontal Decimation Control (MMFF2C)

Read/Write Address: FF2CH
Power-on Default: Undefined

The scheme described below is used if MMFF00_7 = 0 . If MMFF00_7 = 1, the decimation scheme described in Section 12-5 is used.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO DATA BYTE MASK															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VIDEO DATA BYTE MASK															

Bits 31-0 Video Data Byte Mask

Each 32 bytes of video data input is compared with this mask. If a bit in this mask is 1, the corresponding byte is discarded. If a bit is a 0, the corresponding byte is passed to the video memory. In Video 16 mode, each bit masks 2 bytes. In pass-through mode, each bit masks 4 bytes. Normally, decimation starts with bit 0 after an HSYNC. If a horizontal video data offset is specified in MMFF28_11-0 (video 8 or 16 modes only), decimation aligns with the start of data after the offset.

LPB Vertical Decimation Control (MMFF30)

Read/Write Address: FF30H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO DATA LINE MASK															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VIDEO DATA LINE MASK															

Bits 31-0 Video Data Line Mask

Each 32 lines of video data input is compared with this mask. If a bit in the mask is 0, the corresponding line is passed to video memory. If a bit is a 1, the corresponding line is discarded. If a vertical video data offset is specified in MMFF28_24-16 (video 8 or 16 modes only), decimation does not align with the starting line after the offset and instead starts from VSYNC.

LPB Line Stride (MMFF34)

Read/Write Address: FF34H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	LINE STRIDE											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 11-0 Line Stride

Value = byte offset of vertically adjacent pixels

This offset is added to the line starting address each HSYNC to get the new line starting address. Each line must begin on an 8-byte boundary.

Bits 31-12 Reserved

LPB Output FIFO (MMFF40)

Read/Write Address: FF40H, FF44H...,FF5CH
Power-on Default: 00000000H

Writes to any of the addresses in this 8 doubleword address range will be transferred to the LPB input FIFO. This allows efficient use of the MOVSD assembly language instruction. Accesses must be to doubleword addresses.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUT FIFO DATA															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUT FIFO DATA															

Bits 31-0 Output FIFO Data

Note: Software must never transfer more compressed data than there is room for in the output FIFO. This information is read from MMFF04_3-0.

Section 24: PCI Register Descriptions

The PCI specification defines a configuration register space. These registers allow device relocation, device independent system address map construction and automatic configurations. The chip provides a subset of these registers, which are described below.

The configuration register space occupies 256 bytes. When a configuration read or write command is issued, the AD[7:0] lines contain the address of the register in this space to be accessed. The chip supports or returns 0 for the first 64 bytes of this space.

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined).

Vendor ID

Read Only Address: 00H
Power-On Default: 5333H

This read-only register identifies the device manufacturer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vendor ID															

Bits 15-0 Vendor ID
This is hardwired to 5333H to identify S3 Incorporated.

Device ID

Read Only Address: 02H
Power-On Default: 8C01H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device ID															

Bits 15-0 Device ID

Hardwired to 8C01H

Command

Read/Write Address: 04H
Power-On Default: 0000H

This register controls which types of PCI cycles ViRGE/MX can generate and respond to.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	DAC SNP	R	R	BME	MEM	I/O

Bit 0 I/O - Enable Response to I/O Accesses
0 = Response to I/O space accesses is disabled
1 = Response to I/O space accesses enabled

Bit 1 MEM - Enable Response to Memory Accesses
0 = Response to memory space accesses is disabled
1 = Response to memory space accesses enabled

Bit 2 BME - Bus Master Operation Enable
0 = Bus master operation disabled
1 = Bus master operation enabled

Bit 3 Reserved

Bit 4 CL - Capabilities List (Read Only)

This bit is hardwired to 1 to indicate a capabilities list is implemented. PCI34_7-0 point to the first item in the capabilities list.

Bit 5 DAC SNP - RAMDAC Register Access Snooping
0 = ViRGE/MX claims and responds to all RAMDAC register access cycles
1 = ViRGE/MX performs RAMDAC register writes but does not claim the PCI cycle. RAMDAC register read accesses are performed by ViRGE/MX.

Bits 15-6 Reserved

Status

Read/Write Address: 06H
Power-On Default: 0200H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	RMA	RTA	R	DEVSEL		R	R	R	R	R	R	R	R	R

Bits 8-0 Reserved

Bits 10-9 DEVSEL - Device Select Timing
01 = Medium DEVSEL timing. (hardwired)

Bit 11 Reserved

Bit 12 RTA - Received Target Abort
0 = No effect
1 = Bus master transaction terminated with target-abort

This bit is reset by software by writing a 1 to this location.

Bit 13 RMA - Received Master Abort
0 = No effect
1 = Bus master transaction terminated with master-abort

This bit is reset by software by writing a 1 to this location.

Bits 15-14 Reserved

Class Code

Read Only Address: 08H
Power-On Default: 3000000xxH

This register is hardwired to 300000xxH to specify that ViRGE/MX is a VGA-compatible display controller. The xx will change with each revision.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROGRAMMING INTERFACE								REVISION ID							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASE CLASS CODE								SUB-CLASS							

Latency Timer

Read/Write Address: 0DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
BM LATENCY TIMER					0	0	0

Bits 2-0 Reserved = 0

These are the 3 lsb's of the latency timer value, providing 8 clocks granularity.

Bits 7-3 BM LATENCY TIMER - Bus Master Latency Timer

Value = number of PCI clocks ViRGE/MX can keep its bus master grant without having it removed

These are the 5 msb's of this value. The three lsb's are 000b. This value is normally programmed by the system BIOS based in part on the requested value in bits 15-8 of 3EH.

Base Address 0

Read/Write Address: 12H (high) 10H (low)
Power-On Default: 7000 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	PREF = 0	TYPE =00		MSI = 0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASE ADDRESS 0						R	R	R	R	R	R	R	R	R	R

Bit 0 MSI - Memory Space Indicator
0 = Base registers map into memory space (hardwired)

Bits 2-1 TYPE - Type of Address Relocation
00 = Locate anywhere in 32-bit address space (hardwired)

Bit 3 PREF - Prefetchable
0 = Does not meet the prefetchable requirements (hardwired)

Bits 22-4 Reserved

Bits 31-26 BASE ADDRESS 0

Value = upper 6 bits of the base address for accessing ViRGE/MX registers and memory via memory-mapped I/O

This field provides for address relocation. These bits map to system address bits 31-26. All other address bits (25-4) return 0 on read to specify that ViRGE/MX requires a 64 MByte address space. Note that writes to CR59_7-2 will also update this field, so if the linear addressing base address is being changed, the programmer must do a read-modify-write to ensure that this field is not changed.

PCI Configuration Space Subsystem ID

Read Only Address: 2CH
Power-On Default: 00000000H

This register is a shadow of CR95-CR98.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBSYSTEM VENDOR ID															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SUBSYSTEM ID															

Bits 15-0 SUBSYSTEM VENDOR ID

Bits 31-16 SUBSYSTEM ID

BIOS ROM Base Address

Read/Write Address: 32H (high) 30H (low)
Power-On Default: 000C 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	ADE
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BIOS ROM BASE ADDRESS															

Bit 0 ADE - Address Decode Enable
0 = Accesses to the BIOS ROM address space defined in this register are disabled
1 = Accesses to the BIOS ROM address space defined in this register are enabled

Bits 15-1 Reserved

Bits 31-16 BIOS ROM BASE ADDRESS
These are the upper 16 bits of the BIOS ROM address.

Power Management Capabilities List Pointer

Read/Write Address: 34H
Power-On Default: DCH

This register value points to the offset of the first item in the power management capabilities list. It is available only with the 86C261.

7	6	5	4	3	2	1	0
POWER MANAGEMENT CAPABILITIES LIST POINTER							

Bits 7-0 POWER MANAGEMENT CAPABILITIES LIST POINTER

This field is hardwired to DCH.

Interrupt Line

Read/Write Address: 3CH
Power-On Default: 00H

This register contains interrupt line routing information written by the POST program during power-on initialization.

7	6	5	4	3	2	1	0
INTERRUPT LINE							

Bits 7-0 INTERRUPT LINE

Interrupt Pin

Read Only Address: 3DH
Power-On Default: See below.

This register defaults to a value of 00H on reset to specify that no interrupt line is requested. If CR36_0 = 0, this register reads 01H, indicating that INTA is the interrupt pin used.

7	6	5	4	3	2	1	0
INTERRUPT PIN							

Bits 7-0 INTERRUPT PIN

Latency/Grant

Read Only Address: 3EH
Power-On Default: FF04H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXIMUM LATENCY								MINIMUM GRANT							

Bits 7-0 MINIMUM GRANT

Value = Length of burst period required in units of 250 ns (33 MHz clock)

Bits 15-8 MAXIMUM LATENCY

Value = Maximum latency of PCI access in units of 250 ns (33 MHz clock)

PCI Power Management Capability Identifier

Read Only Address: DCH (PM offset + 00H)
Power-On Default: 0001H

This register is only available with the 86C261.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT POINTER								CAPABILITIES ID							

Bits 7-0 CAPABILITIES ID

Hardwired to 01H to identify the capabilities list as pertaining to PCI power management.

Bits 15-8 NEXT POINTER

Hardwired to 00H (no additional capabilities)

PCI Power Management Capabilities

Read Only Address: DEH (PM offset + 02H
Power-On Default: 0000H

This register is only available with the 86C261.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	D2	D1	R	R	R	DSI	R	R	VERSION		

Bits 2-0 VERSION

Hardwired to 1H to indicate compliance with Revision 1.0 of the PCI Power Management Specification.

Bits 4-3 Reserved

Bit 5 DSI - Device Specific Initialization

Hardwired to 1 to indicate a device specific initialization sequence is required following transition to the D0 uninitialized state.

Bits 8-6 Reserved

Bit 9 D1

Hardwired to 1 to indicated support for the D1 power management state.

Bit 10 D2

Hardwired to 1 to indicated support for the D2 power management state.

Bits 15-11 Reserved

PCI Power Management Control/Status

Read Only (unless noted) Address: E0H (PM offset + 04H
Power-On Default: 0000H

This register is only available with the 86C261.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	PS	

Bits 1-0 PS - Power State (Read/Write)
00 = D0
01 = D1
10 = D2
11 = $D3_{hot}$

Bits 15-2 Reserved

Section 25: TV Register Descriptions

The following registers are located in Sequencer Register address space not used by standard VGA. An appropriate value must be programmed in SR8 to unlock access to these registers.

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). See Appendix A for a table listing each register in this section and its page number.

TV Flicker Filter Control 1 Register (SR70)

Read/Write Address: 3C5H, Index 70H
Power-On Default: 00H

7	6	5	4	3	2	1	0
OFF	SSFF	R	AAS	CFC	CCSS	FFM	FFE

Bit 0 FFE - TV Flicker Filter Enable
0 = Flicker filter disabled
1 = Flicker filter enabled

The timing of the enable is controlled by SR86_7. This bit must also be set to 1 to enable conversion to interlaced output.

Bit 1 FFM - TV Flicker Filter Method
0 = 3-line flicker filter
1 = 2-line flicker filter

Bit 2 CSCC - Color Space Conversion Control
0 = Convert pixels to 4:2:2 YCbCr format. Up to 720 pixels/line can be supported. The number of horizontal active pixels musts be divisible by 8.
1 = Convert pixels to 4:1:1 YCbCr format. Up to 900 pixels/line can be supported. The number of horizontal active pixels must be divisible by 10.

Bit 3 CFC - Chroma Filter Control
0 = Chroma filter enabled. Cb and Cr components are filtered after conversion from RGB to YCbCr.
1 = Chroma filter disabled. Cb and Cr components are subsampled after conversion from RGB to YCbCr.

Bit 4 AAS - Active Area Select
0 = Invert of horizontal $\overline{\text{BLANK}}$ is used to generate active area
1 = Horizontal Display Enable is used to generate active area

The = 0 setting captures the border area but has more pixels/line. If the data does not fit in the line buffer, the = 1 setting can be used.

Bit 5 SSFF - Secondary Stream Flicker Filter
0 = Disable flicker filter for secondary stream
1 = Enable flicker filter for secondary stream

Note that the secondary window must be positioned at an even pixel boundary if input data is converted to 4:2:2 YCbCr or at a quad pixel boundary if input data is converted to 4:1:1 YCbCr.

Bit 6 Reserved

Bit 7 OFF - Output Flicker Filter on CRT DAC
0 = CRT DAC is used to output CRT data
1 = CRT DAC is used to output flicker filter data

The = 1 option supports use of an external TV encoder. The chrominance value is converted from a signed to an unsigned value.

TV Flicker Filter Control 2 Register (SR71)

Read/Write Address: 3C5H, Index 71H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	CCO	LO	LC	R	FILTER FRACT		

Bits 2-0 FILTER FRACT - Filtering Fraction (f)
000 = f = 9/16 for 2-line filter and reserved for 3-line filter
001 = f = 10/16 for 2-line filter and reserved for 3-line filter
010 = f = 11/16 for 2-line filter and f = 6/16 for 3-line filter
011 = f = 12/16 for 2-line filter and f = 8/16 for 3-line filter
100 = f = 13/16 for 2-line filter and f = 10/16 for 3-line filter
101 = f = 14/16 for 2-line filter and f = 12/16 for 3-line filter
110 = f = 15/16 for 2-line filter and f = 14/16 for 3-line filter
111 = f = 16/16. No filtering is done in this case. However, conversion of non-interlaced data to interlaced data is still performed.

These bits are used when Set Interpolative Threshold (SIT) is not enabled, or when SIT is enabled and the Y difference is greater than or equal to the SIT value specified in SR73.

For a 2-line flicker filter: during the even field, even lines are weighted by this fraction (f) and odd lines are weighted by (1-f); similarly during the odd field, odd lines are weighted by this fraction (f) and even lines are weighted by (1-f).

For a 3-line flicker filter: during the even field, even lines are weighted by this fraction (f) and previous/next odd lines are weighted by (1-f); similarly during the odd field, odd lines are weighted by this fraction (f) and previous/next even lines are weighted by (1-f).

Bit 3 Reserved

Bit 4 LC - Luminance Clipping
0 = Y range is 0 to 255
1 = Y is clipped from 0 to 219

Clipping is applied at the output of the TV flicker filter and the = 1 setting is effective only when SR70_0 =1.

Bit 5 LO - Luminance Offset
0 = No offset on Y value
1 = Y is offset by 16

The = 1 setting should be used only if SR71_4 = 1 and it is effective only when SR70_0 = 1.

Bit 6 CCO - Chrominance Clipping Option
0 = Cr and Cb range is -128 to 127
1 = Cr, Cb range is -112 to +112.

The = 1 setting is effective only when SR70_0 = 1.

Bit 7 422 - Enable 8-bit 4:2:2 Output
0 = 8-bit 4:2:2 output disabled
1 = See description of SR30_7 when set to 1.

TV Flicker Filter Control 3 Register (SR72)

Read/Write Address: 3C5H, Index 72H
Power-On Default: 00H

7	6	5	4	3	2	1	0
FTM2	FTM1	CTM		ACC		SIT	YFO

Bit 0 YFO - Y Filter Only
0 = Flicker filter is applied to Y, Cr, Cb components
1 = Flicker filter is applied to Y component only

Bit 1 SIT - Set Interpolative Threshold (SIT) Enable
0 = SIT disabled
1 = SIT enabled

Bits 3-2 ACC - Aperture/Inverse Aperture Correction Control
00 = Aperture/Inverse aperture correction disabled
01 = Aperture correction enabled
10 = Inverse aperture correction enabled
11 = Reserved

Aperture/Inverse aperture correction is applied only on the Y component.

Bits 5-4 CTM - CRT/TV Test Mode Select

These bits for S3 testing only and are effective only when SR31_0 = 1.

Bit 6 FTM1 - Flicker Filter Test Mode Enable 1
0 = Flicker filter test mode 1 disabled
1 = Flicker filter test mode 1 enabled

This bit is for S3 testing only.

Bit 7 FTM2 - Flicker Filter Test Mode Enable 2
0 = Flicker filter test mode 2 disabled
1 = Flicker filter test mode 2 enabled.

This bit is for S3 testing only.

Set Interpolative Threshold Register (SR73)

Read/Write Address: 3C5H, Index 73H
Power-On Default: 00H

7	6	5	4	3	2	1	0
SIT							

Bits 7-0 Set Interpolative Threshold (SIT) Value

During flicker filtering, this value is compared to the Y difference of the primary pixel and the vertically adjacent pixel(s). If the difference is greater than or equal to this value, then SR71_2-0 is used to filter the Y, Cb, and Cr components. Otherwise, if the difference is less than this value, then no vertical filtering will be performed.

Aperture Correction Register (SR74)

Read/Write Address: 3C5H, Index 74H
Power-On Default: 00H

7	6	5	4	3	2	1	0
APERTURE CORRECTION							

Bits 7-0 Aperture Correction (AC) Value

This value is used to offset (add to/subtract from) the Y value depending on the magnitude of the Y value and depending on SR72_3-2. The Cb and Cr components are not affected by aperture correction.

Aperture Correction Low Threshold Register (SR75)

Read/Write Address: 3C5H, Index 75H
Power-On Default: 00H

7	6	5	4	3	2	1	0
APERTURE CORRECTION LOW THRESHOLD							

Bits 7-0 Aperture Correction Low (ACL) Threshold Value

Aperture Correction Mid Threshold Register (SR76)

Read/Write Address: 3C5H, Index 76H
Power-On Default: 00H

7	6	5	4	3	2	1	0
APERTURE CORRECTION MID THRESHOLD							

Bits 7-0 Aperture Correction Mid (ACM) Threshold Value

Aperture Correction High Threshold Register (SR77)

Read/Write Address: 3C5H, Index 77H
Power-On Default: 00H

7	6	5	4	3	2	1	0
APERTURE CORRECTION HIGH THRESHOLD							

Bits 7-0 Aperture Correction High (ACH) Threshold Value

TV VSYNC Delay Register (SR78)

Read/Write Address: 3C5H, Index 78H
Power-On Default: 00H

7	6	5	4	3	2	1	0
TV VSYNC DELAY BITS 11-4							

Bits 7-0 TV VSYNC Delay Bits 11-4

12-bit Value = the amount of VSYNC delay (in pixel clock periods) of the controller which drives the TV

The 4 least significant bits of this value are hardwired to 0000b. Flicker filter output is at DCLK/2. The HSYNC output is halved, but not the VSYNC, which puts them out of phase. This field is used to re-align the active edges of the two signals.

U-Burst Register (SR79)

Read/Write Address: 3C5H, Index 79H
Power-On Default: 00H

7	6	5	4	3	2	1	0
U-BURST							

Bits 7-0 U-BURST<$IU/V color burst

Value = U-burst for NTSC/PAL

If SR19_4 = 1, the value programmed in this register is used to generate the AY output for DAC sense use.

V-Burst Register (SR7A)

Read/Write Address: 3C5H, Index 7AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
V-BURST							

Bits 7-0 V-BURST

Value = V-burst for NTSC/PAL

If SR19_4 = 1, the value programmed in this register is used to generate the AC output for DAC sense use.

Subcarrier to Pixel Clock Ratio 1 Register (SR7B)

Read/Write Address: 3C5H, Index 7BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
SUBCARRIER TO PIXEL CLOCK RATIO BITS 7-0							

Bits 7-0 SUBCARRIER TO PIXEL CLOCK RATIO BITS 7-0

20-bit Value = TV subcarrier frequency/TV encoder pixel clock frequency * 2^{20}

The subcarrier frequency is 3.579545 MHz for NTSC or 4.430 MHz for PAL. The pixel clock for the TV encoder is the programmed DCLK divided by 2 when the TV flicker filter is enabled or DCLK when the TV flicker filter is disabled. In the case when DCLK may be inaccurate, this register can be used to make adjustments to generate the correct subcarrier frequency. Bits 15-8 are in SR7C and bits 19-16 are in SR7D_7-4].

Subcarrier to Pixel Clock Ratio 2 Register (SR7C)

Read/Write Address: 3C5H, Index 7CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
SUBCARRIER TO PIXEL CLOCK RATIO BITS 15-8							

Bits 7-0 SUBCARRIER TO PIXEL CLOCK RATIO BITS 15-8

20-bit Value = TV subcarrier frequency/TV encoder pixel clock frequency * 2^{20}

See the description of SR7B.

Underscanning Control 1 Register (SR7D)

Read/Write Address: 3C5H, Index 7DH
Power-On Default: 00H

Bits 0, 2 and 3 of this register along with SR7E and SR7F control vertical underscanning, which can be enabled only in graphics modes. When underscanning is enabled, the position of the hardware icon and cursor must be adjusted by software whether or not underscanning is enabled for them. Also, the position and size of the secondary stream window must also be adjusted by software. Underscanning therefore should only be used in 480-line VGA-compatible mode (e.g., mode 12) where the hardware cursor and secondary stream are not being used. A lower vertical resolution graphics mode can be used instead of underscanning to allow use of the cursor, icon and secondary stream without adjustments.

7	6	5	4	3	2	1	0
SUB TO PIX RATIO BITS 19-16				EUI	EUC	F8	UM

Bit 0 UM - Underscanning Method
0 = Delete different lines in even and odd fields
1 - Delete same lines in even and odd fields

Bit 1 F8 - Force 8-dot Text
0 = 9-dot text is not forced to 8-dot text
1 = 9-dot text is forced to 8-dot text

If this bit is set to 1 in text mode, 640-dot parameters must be used instead of 720-dot parameters.

Bit 2 EUC - Enable Underscanning for Cursor
0 = Disable underscanning on hardware cursor
1 = Enable underscanning on hardware cursor

Bit 3 EUI - Enable Underscanning for Icon
0 = Disable underscanning on icon
1 = Enable underscanning on icon

Bits 7-4 SUBCARRIER TO PIXEL CLOCK RATIO BITS 19-16

20-bit Value = TV subcarrier frequency/TV encoder pixel clock frequency * 2^{20}

See the description of SR7B.

Underscanning Control 2 Register (SR7E)

Read/Write Address: 3C5H, Index 7EH
Power-On Default: 00H

This register controls vertical underscanning, which can be enabled only in graphics modes.

7	6	5	4	3	2	1	0
UNDERSCANNING INTERVAL				UESP			

Bits 3-0 UESP - Underscanning Enable and Start Position

When these bits are programmed to non-zero value, they normally specify the first line number that will be deleted for underscanning. The exception is for the odd field when SR7D_0 = 1, in which case the first line number that will be deleted is specified by this value + 1.

When these bits are programmed to 0H, underscanning is disabled. Consequently, line 0 cannot be the first line that is deleted. Note that underscanning affects graphics modes only and it is always disabled in text modes.

Bits 7-4 UNDERSCANNING INTERVAL

Value = the interval between deleted lines when underscanning is enabled

Underscanning Control 3 Register (SR7F)

Read/Write Address: 3C5H, Index 7FH
Power-On Default: 00H

This register controls vertical underscanning, which can be enabled only in graphics modes.

7	6	5	4	3	2	1	0
UNDERSCANNING OFFSET							

Bits 7-0 UNDERSCANNING OFFSET

Value= the number of deleted lines/frame when underscanning is enabled (SR7E_3-0 are not 0H).

Color Space Converter Factor 0 Register (SR80)

Read/Write Address: 3C5H, Index 80H
Power-On Default: 00H

7	6	5	4	3	2	1	0
COLOR SPACE CONVERTER FACTOR 0 (f_0)							

Bits 7-0 COLOR SPACE CONVERTER FACTOR 0 (f_0)

Value = 512 * red color weighting factor for calculating the Y component

The CCIR 601 standard is 1000 0011b.

Color Space Converter Factor 1 Register (SR81)

Read/Write Address: 3C5H, Index 81H
Power-On Default: 00H

7	6	5	4	3	2	1	0
COLOR SPACE CONVERTER FACTOR 1 (f_1)							

Bits 7-0 COLOR SPACE CONVERTER FACTOR 1 (f_1)

9- bit Value = 512 * green color weighting factor for calculating the Y component

Bit 8 of this value is SR82_7. The CCIR 601 standard is 1 0000 0010b.

Color Space Converter Factor 2 Register (SR82)

Read/Write Address: 3C5H, Index 82H
Power-On Default: 00H

7	6	5	4	3	2	1	0
F18	R	COLOR SPACE CONVERTER FACTOR 2 (f_2)					

Bits 5-0 COLOR SPACE CONVERTER FACTOR 2 (f_2)

Value = 512 * blue color weighting factor for calculating the Y component

The CCIR 601 standard is 11 0010b.

Bit 6 Reserved

Bit 7 F18 - Bit 8 of the f_1 Color Space Converter Factor

Color Space Converter Factor 3 Register (SR83)

Read/Write Address: 3C5H, Index 83H
Power-On Default: 00H

7	6	5	4	3	2	1	0
COLOR SPACE CONVERTER FACTOR 3 (f_3)							

Bits 7-0 COLOR SPACE CONVERTER FACTOR 3 (f_3)

Value = 512 * red color weighting factor for calculating the Cr component

The CCIR 601 standard is 1110 0001b.

Color Space Converter Factor 4 Register (SR84)

Read/Write Address: 3C5H, Index 84H
Power-On Default: 00H

7	6	5	4	3	2	1	0
COLOR SPACE CONVERTER FACTOR 4 (f_4)							

Bits 7-0 COLOR SPACE CONVERTER FACTOR 4 (f_4)

Value = 512 * green color weighting factor for calculating the Cr component

The CCIR 601 standard is 1011 1100b.

Color Space Converter Factor 5 Register (SR85)

Read/Write Address: 3C5H, Index 85H
Power-On Default: 00H

7	6	5	4	3	2	1	0
BCSC	R	COLOR SPACE CONVERTER FACTOR 5 (f_5)					

Bits 5-0 COLOR SPACE CONVERTER FACTOR 5 (f_5)

Value = 512 * blue color weighting factor for calculating the Cr component

The CCIR 601 standard is 10 0101b.

Bit 6 Reserved

Bit 7 BSCS - Bypass Color Space Conversion
0 = Normal operation
1 = Pass RGB data unchanged

This bit is used only for S3 testing.

Color Space Converter Factor 6 Register (SR86)

Read/Write Address: 3C5H, Index 86H
Power-On Default: 00H

7	6	5	4	3	2	1	0
FFES	COLOR SPACE CONVERTER FACTOR 6 (f_6)						

Bits 6-0 COLOR SPACE CONVERTER FACTOR 6 (f_6)

Value = 512 * red color weighting factor for calculating the Cb component

The CCIR 601 standard is 100 1100b.

Bit 7 FFES - Flicker Filter Enable Select
0 = SR70_0 is effective immediately when programmed
1 = SR70_0 is effective at the next VSYNC after it is programmed

Color Space Converter Factor 7 Register (SR87)

Read/Write Address: 3C5H, Index 87H
Power-On Default: 00H

7	6	5	4	3	2	1	0
COLOR SPACE CONVERTER FACTOR 7 (f_7)							+

Bits 7-0 COLOR SPACE CONVERTER FACTOR 7 (f_7)

Value = 512 * green color weighting factor for calculating the Cb component

The CCIR 601 standard is 1001 0101b.

Color Space Converter Factor 8 Register (SR88)

Read/Write Address: 3C5H, Index 88H
Power-On Default: 00H

7	6	5	4	3	2	1	0
COLOR SPACE CONVERTER FACTOR 8 (f_8)							

Bits 7-0 COLOR SPACE CONVERTER FACTOR 8 (f_8)

Value = 512 * blue color weighting factor for calculating the Cb component

The CCIR 601 standard is 1110 0001b.

Software Scratch 0 Register (SR89)

Read/Write Address: 3C5H, Index 89H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved for Use by S3 Software

Software Scratch 1 Register (SR8A)

Read/Write Address: 3C5H, Index 8AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved for Use by S3 Software

Software Scratch 2 Register (SR8B)

Read/Write Address: 3C5H, Index 8BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved for Use by S3 Software

Software Scratch 3 Register (SR8C)

Read/Write Address: 3C5H, Index 8CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved for Use by S3 Software

Software Scratch 4 Register (SR8D)

Read/Write Address: 3C5H, Index 8DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved for Use by S3 Software

Software Scratch 5 Register (SR8E)

Read/Write Address: 3C5H, Index 8EH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved for Use by S3 Software

Software Scratch 6 Register (SR8F)

Read/Write Address: 3C5H, Index 8FH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Bits 7-0 Reserved for Use by S3 Software

TV Parameter 0 Register (SR90)

Read/Write Address: 3C5H, Index 90H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TV PARAMETER 0							

Bits 7-0 Start of TV HSYNC Pulse/Start of First Equalizing Pulse/End of Second Serration Pulse

11-bit Value = the above TV parameters from the rising edge of internal HSYNC in terms of TV pixel clock periods

Bits 11-8 are SR9B_3-0. The BIOS should program this register to 00H after reset.

TV Parameter 1 Register (SR91)

Read/Write Address: 3C5H, Index 91H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TV PARAMETER 1							

Bits 7-0 End of First Equalizing Pulse

11-bit Value = the above TV parameter from the rising edge of internal HSYNC in terms of TV pixel clock periods

Bits 11-8 are SR9B_6-4. The BIOS should program this register to 00H after reset.

TV Parameter 2 Register (SR92)

Read/Write Address: 3C5H, Index 92H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TV PARAMETER 2							

Bits 7-0 End of TV HSYNC Pulse

11-bit Value = the above TV parameter from the rising edge of internal HSYNC in terms of TV pixel clock periods

Bits 11-8 are in SR9C_2-0. The BIOS should program this register to 00H after reset.

TV Parameter 3 Register (SR93)

Read/Write Address: 3C5H, Index 93H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TV PARAMETER 3							

Bits 7-0 Start of Burst Flag Pulse

11-bit Value = the above TV parameter from the rising edge of internal HSYNC in terms of TV pixel clock periods

Bits 11-8 are in SR9C_6-4. The BIOS should program this register to 00H after reset.

TV Parameter 4 Register (SR94)

Read/Write Address: 3C5H, Index 94H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TV PARAMETER 4							

Bits 7-0 End of Burst Flag Pulse

11- bit Value = the above TV parameter from the rising edge of internal HSYNC in terms of TV pixel clock periods

Bits 11-8 are in SR9D_2-0. The BIOS should program this register to 00H after reset.

TV Parameter 5 Register (SR95)

Read/Write Address: 3C5H, Index 95H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TV PARAMETER 5							

Bits 7-0 Start of Active Video Line

11-bit Value = the above TV parameter from the rising edge of internal HSYNC in terms of TV pixel clock periods

Bits 11-8 are in SR9D_6-4. The BIOS should program this register to 00H after reset.

TV Parameter 6 Register (SR96)

Read/Write Address: 3C5H, Index 96H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TV PARAMETER 6							

Bits 7-0 Start of First Serration Pulse

10-bit Value = the above TV parameter from the rising edge of internal HSYNC in terms of TV pixel clock periods

Bits 9-8 are SR9E_1-0. The BIOS should program this register to 00H after reset.

TV Parameter 7 Register (SR97)

Read/Write Address: 3C5H, Index 97H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TV PARAMETER 7							

Bits 7-0 End of First Serration Pulse/Start of Second Equalization Pulse

10-bit Value = the above TV parameters from the rising edge of internal HSYNC in terms of TV pixel clock periods

Bits 9-8 are SR9E_3-2. The BIOS should program this register to 00H after reset.

TV Parameter 8 Register (SR98)

Read/Write Address: 3C5H, Index 98H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TV PARAMETER 8							

Bits 7-0 End of Second Equalizing Pulse

10-bit Value = the above TV parameter from the rising edge of internal HSYNC in terms of TV pixel clock periods

Bits 9-8 are SR9E_5-4. The BIOS should program this register to 00H after reset.

TV Parameter 9 Register (SR99)

Read/Write Address: 3C5H, Index 99H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TV PARAMETER 9							

Bits 7-0 Start of Second Serration Pulse

11-bit Value = the above TV parameter from the rising edge of internal HSYNC in terms of TV pixel clock periods

Bits 10-8 are SR9F_2-0. The BIOS should program this register to 00H after reset.

TV Parameter 10 Register (SR9A)

Read/Write Address: 3C5H, Index 9AH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TV PARAMETER 10							

Bits 7-0 End of Active Video Line

11-bit Value = the above TV parameter from the rising edge of internal HSYNC in terms of TV pixel clock periods

Bits 10-0 are SR9F_6-4. The BIOS should program this register to 00H after reset.

TV Overflow Parameter 0 Register (SR9B)

Read/Write Address: 3C5H, Index 9BH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	TV P1 BITS 10-8			R	TV P0 BITS 10-8		

Bits 2-0 TV PARAMETER 0 BITS 10-8

Bits 7-0 are in SR90.

Bit 3 Reserved

Bits 6-4 TV PARAMETER 1 BITS 10-8

Bits 7-0 are in SR91.

Bit 7 Reserved

The BIOS should program this register to 00H after reset.

TV Overflow Parameter 1 Register (SR9C)

Read/Write Address: 3C5H, Index 9CH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	TV P3 BITS 10-8			R	TV P2 BITS 10-8		

Bits 2-0 TV PARAMETER 2 BITS 10-8

Bits 7-0 are in SR92.

Bit 3 Reserved

Bits 6-4 TV PARAMETER 3 BITS 10-8

Bits 7-0 are in SR93

Bit 7 Reserved

The BIOS should program this register to 00H after reset.

TV Overflow Parameter 2 Register (SR9D)

Read/Write Address: 3C5H, Index 9DH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	TV P5 BITS 10-8			R	TV P4 BITS 10-8		

Bits 2-0 TV PARAMETER 4 BITS 10-8

Bits 7-0 are in SR94.

Bit 3 Reserved

Bits 6-4 TV PARAMETER 5 BITS 10-8

Bits 7-0 are in SR95.

Bit 7 Reserved

The BIOS should program this register to 00H after reset.

TV Overflow Parameter 3 Register (SR9E)

Read/Write Address: 3C5H, Index 9EH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	P8 BITS 9-8		P7 BITS 9-8		P6 BITS 9-8	

Bits 1-0 TV PARAMETER 6 BITS 9-8

Bits 7-0 are in SR96.

Bits 3-2 TV PARAMETER 7 BITS 9-8

Bits 7-0 are in SR97.

Bits 5-4 TV PARAMETER 8 BITS 9-8

Bits 7-0 are in SR98.

Bits 7-6 Reserved

The BIOS should program this register to 00H after reset.

TV Overflow Parameter 4 Register (SR9F)

Read/Write Address: 3C5H, Index 9FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TVT2	TV P10 BITS 10-8			TVT1	TV P9 BITS 10-8		

Bits 2-0 TV PARAMETER 9 BITS 10-8

Bits 7-0 are in SR99.

Bit 3 TVT1 - TV Encoder Test Mode 1

This bit is for S3 testing only.

Bits 6-4 TV PARAMETER 10 BITS 10-8

Bits 7-0 are in SR9A.

Bit 7 TVT2 - TV Encoder Test Mode 2

This bit is for S3 testing only.

The BIOS should program this register to 00H after reset.

Section 26: Flat Panel Register Descriptions

The following registers are located in Sequencer Register address space not used by standard VGA. An appropriate value must be programmed in SR8 to unlock access to these registers.

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). See Appendix A for a table listing each register in this section and its page number.

Architecture Configuration Register (SR30)

Read/Write Address: 3C5H, Index 30H
Power-On Default: 00H

7	6	5	4	3	2	1	0
EES	FPTM	R	C2D	C1D	TVS	SPS	PST

Bit 0 PCT - Panel Scan Type
0 = Dual-scan STN panel
1 = TFT or single-scan STN panel

Bit 1 SPS- Streams Processor Source
0 = Streams Processor Source is Controller 1
1 = Streams Processor Source is Controller 2

CLUT 1 is used for the controller sourcing the Streams Processor and CLUT2 is used for the other controller.

Bit 2 TVS - TV DAC Source
0 = TV DAC source is Controller 1
1 = TV DAC source is Controller 2

Either CLUT can be assigned to this DAC, depending on the setting of bit 1 of this register.

Bit 3 C1D = Controller 1 DCLK
0 = Controller 1 uses DCLK1
1 = Controller 1 uses DCLK2

Note that only Controller 1 contains VGA logic. As long as the DCLK driving it (DCLK1 or DCLK2) is only driving Controller 1, the settings of 3C2H_3-2 = 00b (PLL M & N values from SR22/SR23 generating 25.175 MHz) and 3C2H_3-2 = 01b (PLL M & N values from SR24/SR25 generating 28.322 MHz) can be used. This is the default case, with DCLK1 driving Controller 1 and DCLK2 driving Controller 2. If the DCLK driving Controller 1 is also used to drive Controller 2, these settings are invalid because they cannot be used with Controller 2, which has no VGA logic. Therefore in this case with the same DCLK driving both Controllers, the PLL M & N values will be automatically taken from SR12 and SR13 for DCLK1 or SRE and SRF for DCLK2.

Bit 4 C2D - Controller 2 DCLK
0 = Controller 2 uses DCLK2
1 = Controller 2 uses DCLK1

Note that DCLK2 defaults to driving only Controller 2, so its PLL M and N values will initially be taken from SRE and SRF. See the description for SR30_3.

Bit 5 Reserved

Bit 6 FPTM - Flat Panel Test Mode

This bit is reserved for S3 testing

Bit 7 EES - External Encoder Support
0 = FPD[35:24] are used to output flat panel data (assuming SR31_0 = 0)
1 = FPD[35:24] are used to output flicker filter data for 8-bit external encoder support

SR71_7 must be 1 and SR72_5-4 must be 00b when this bit is set to 1. The output format is 8-bit 4:2:2 YCrCb (CCIR656). Data ordering is CbYCrY. EAV and SAV fields are not supported. Data is on FPD[35:28], the flicker filter ODD field flag is on FPD27, the clock is on FPD26, VSYNC is on FPD25 and HSYNC or display enable is on FPD24, depending on SR82_6.

Flat Panel Display Mode Register (SR31)

Read/Write Address: 3C5H, Index 31H
Power-On Default: 00H

7	6	5	4	3	2	1	0
CD	ID	R	FPD	CT	DACS	FPS	CTM

Bit 0 CTM - CRT Test Mode
0 = Standard flat panel operation
1 = CRT test mode (reserved for S3 use)

Bit 1 FPS - Flat Panel Data Source
0 = Controller 1 is flat panel source
1 = Controller 2 is flat panel source

This bit is valid only if SR31_0 = 0.

Bit 2 DACS - CRT DAC Source Select
0 = Controller 1 is CRT DAC source
1 = Controller 2 is CRT DAC source

Either CLUT can be assigned to this DAC, depending on the setting of bit 1 of SR30.

Bit 3 BLUT - Bypass CLUT Test Mode
0 = Normal operation
1 = Force bypass of Controller 1 and Controller 2 CLUTs in all modes

This bit is for test purposes only.

Bit 4 FPE - Flat Panel Display Enable
0 = Disable flat panel display
1 = Enable flat panel display

Setting this bit to 1 triggers a panel power-on sequence and turns on the clocks to the flat panel logic. Clearing this bit to 0 triggers a panel power-down sequence and disables the clocks to the flat panel logic.

Bit 5 Reserved

Bit 6 ID - Icon Destination Select
0 = Hardware icon controlled by controller 1
1 = Hardware icon controlled by controller 2

The hardware icon is available in any video mode. This bit determines on which screen the icon will appear in dual image mode (both controllers being used).

Bit 7 CD - Cursor Destination Select
0 = Hardware cursor controlled by controller 1
1 = Hardware cursor controlled by controller 2

The hardware cursor is only available in Enhanced mode (not VGA). This bit determines on which screen the cursor will appear in dual display mode (both controllers being used).

Flat Panel Polarity Control Register (SR32)

Read/Write Address: 3C5H, Index 32H
Power-On Default: 00H

7	6	5	4	3	2	1	0
VSP	HSP	DEP	FPDP	FP	CVSP	CHSP	R

Bit 0 Reserved

Bit 1 CHSP - CRT HSYNC Polarity During Simultaneous Display
0 = HSYNC polarity is active high
1 = HSYNC polarity is active low

This bit controls HSYNC polarity (instead of 3C2H_6 Write Only) when simultaneous display is used (SR31_4 = 1 AND SR31_1 = SR31_2).

Bit 2 CVSP - CRT VSYNC Polarity During Simultaneous Display
0 = VSYNC polarity is active high
1 = VSYNC polarity is active low

This bit controls VSYNC polarity (instead of 3C2H_7 Write Only) when simultaneous display is used (SR31_4 = 1 AND SR31_1 = SR31_2).

Bit 3 FP - FPDCLK Polarity
0 = Active high
1 = Active low

Bit 4 FPDP - Flat Panel Data Polarity
0 = Active high
1 = Active low

Bit 5 DEP - FPDE Polarity
0 = Active high
1 = Active low

Bit 6 HSP - FPHSYNC Polarity
0 = Active high
1 = Active low

For STN panels, this is the LP signal.

Bit 7 VSP - FPVSYNC Polarity
0 = Active high
1 = Active low

For STN panels, this is the FLM signal.

Flat Panel Function Control 1 Register (SR33)

Read/Write Address: 3C5H, Index 33H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	ELP	HCIE	8FF	FPDCLK DELAY			FOE

Bit 0 FOE - FPDCLK Output Enable
0 = FPDCLK output disabled
1 = FPDCLK output enabled

Bits 3-1 FPDCLK DELAY

Value = FPDCLK delay in ns (typical)

This bit is effective only when FPGPIO is an output.

Bit 4 8FF - Force 8 Frame FRC
0 = FRC rate specified by SR39
1 = When the secondary stream is output to an STN panel, 8 frame FRC is forced.

Bit 5 HCIE - Hardware Cursor/Icon Enable During Screen Off
0 = Hardware cursor and icon disabled during screen off
1 = Hardware cursor and icon enabled during screen off

Bit 6 ELP - Extra LP Enable
0 = Normal LP
1 = Add an extra LP for STN panel when LP is disabled during vertical blanking

LP is disabled during vertical blanking via SR3D_4 = 1.

Bit 7 Reserved

Flat Panel AC Modulation Register (SR34)

Read/Write Address: 3C5H, Index 34H
Power-On Default: 00H

This register only applies to STN panels that require a MOD input.

7	6	5	4	3	2	1	0
ME	MODULATION PERIOD						

Bits 6-0 MODULATION PERIOD

Value = (width of MOD pulse in clock period units) - 1

The clock units (line or frame) are selected via SR35_4.

Bit 7 ME - Modulation Enable
0 = Pin B15 is FPDE
1 = Enable output of MOD signal on pin B15

Flat Panel Function Control 2 Register (SR35)

Read/Write Address: 3C5H, Index 35H
Power-On Default: 00H

7	6	5	4	3	2	1	0
GTM2	TM2	TM1	MODC	FD	FPGPIO SELECT		

Bits 2-0 FPGPIO SELECT
000 = FPGPIO output buffer is tristated and input buffer disabled
001 = Output bit 3 of this register on FPGPIO pin
010 = Output FPDCLK on FPGPIO pin
011 = Output MCLK on FPGPIO pin
100 = Output Controller 1 DCLK on FPGPIO pin
101 = Output Controller 2 DCLK on FPGPIO pin
110 = Output panel on signal. Active high indicates flat panel data and control signals are active
111 = FPGPIO is an input and is read through bit 3 of this register.

Bit 3 FD - FPGPIO Data

If SR35_2-0 = 001b, the state of this bit is output on the FPGPIO pin. If SR35_2-0 = 111b, the FPGPIO pin is an input and its state is read via this bit.

Bit 4 MODC - MOD Clock Select
0 = Line clock
1 = Frame clock

Bit 5 TM1 - Flat Panel Test Mode 1
0 = Normal operation
1 = Test mode 1 (reserved for S3 use)

Bit 6 TM2 - Flat Panel Test Mode 2
0 = Normal operation
1 = Test mode 2 (reserved for S3 use)

Bit 7 GTM2 - General Test Mode 2
0 = Normal operation
1 = Test mode (reserved for S3 use)

Flat Panel Dither Control Register (SR36)

Read/Write Address: 3C5H, Index 36H
Power-On Default: 00H

7	6	5	4	3	2	1	0
DTR CON		DTR BASE COLOR			DTR BIT SELECT		

Bit 0 DBS - Dither Bit Select
0 = 2 bits selected (2x2 dither pattern)
1 = 4 bits selected (4x4 dither pattern)

Bits 2-1 Reserved

Bits 5-3 DTR BASE COLOR
000 = 8 bits selected (no dithering)
001 = Reserved
010 = Reserved
011 = 3 bits selected
100 = 4 bits selected
101 = 5 bits selected
110 = 6 bits selected
111 = Reserved

Bits 7-6 DTR CON - Dither Control
00 = Dithering disabled
01 = Dithering in all modes
10 = Dither in graphics modes (not text)
11 = Dither in graphics modes with 8 bpp or more color

Flat Panel FRC Weight Select RAM Pointer Register (SR37)

Read/Write Address: 3C5H, Index 37H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	WEIGHT SELECT POINTER			

Bits 3-0 WEIGHT SELECT POINTER

Value = offset from the base address of the weight decoding RAM

Bits 7-4 Reserved

Flat Panel FRC Weight Select RAM Data Register (SR38)

Read/Write Address: 3C5H, Index 38H
Power-On Default: 00H

7	6	5	4	3	2	1	0
WEIGHT SELECT DATA							

Bits 7-0 WEIGHT SELECT DATA

The actual value will be supplied by S3 for specific panels.

Flat Panel FRC Control Register (SR39)

Read/Write Address: 3C5H, Index 39H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	FRC GRAY		R	PANEL TYPE	

Bit 1-0 PANEL TYPE
00 = TFT panel
01 = Reserved
10 = STN panel. This setting enables FRC operation.
11 = Reserved

Bit 2 Reserved

Bits 4-3 FRC GRAY - Frame Rate Control Gray Level Select
00 = 16 levels
01 = 8 levels
10 = Reserved
11 = Reserved

Bit 7-5 Reserved

Flat Panel FRC Tuning 1 Register (SR3A)

Read/Write Address: 3C5H, Index 3AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
TUNING DATA 15-8							

The actual value will be supplied by S3 for specific panels. This is the Most Significant Byte of the tuning data.

Flat Panel FRC Tuning 2 Register (SR3B)

Read/Write Address: 3C5H, Index 3BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
TUNING DATA 7-0							

The actual value will be supplied by S3 for specific panels. This is the Least Significant Byte of the tuning value.

Flat Panel Test Register (SR3C)

Read/Write Address: 3C5H, Index 3CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	STN	R	R

Bits 1-0 Reserved = 11 (STN panel operation)

The BIOS should set these bits to 11 for STN panel operaton.

Bit 2 STM - STN Test Mode
0 = Normal operation
1 = STN Test Mode

This test mode is reserved for factory testing.

Bits 7-3 Reserved

Flat Panel Configuration Register (SR3D)

Read/Write Address: 3C5H, Index 3DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
SCDS	FPDS	SCS	LPS	CFGS	FP DATA FORMAT		

Bits 2-0 FP DATA FORMAT
000 = 16-bit STN; 1 pixel/clock TFT (9-, 12-, 15- or 18-bit)
001 = 8-bit STN; 1 pixel/clock TFT (24-bit)
010 = 24-bit STN; 2 pixels/clock TFT (2x9-bit, 2x12-bit, 2x15, 2x18-bit)

All other values are reserved. The STN definition applies if SR39_1-0 = 10b and the TFT definition applies if SR39_1-0 = 00b.

Bit 3 CFGS - Pin Configuration Select for Flat Panel Data Signals
0 = Pin configuration shown in Tables 11-1 and 11-3
1 = Pin configuration shown in Tables 11-2 and 11-4

Bit 4 LPS - LP Stop (STN panels only)
0 = LP and FPSCLK enabled during vertical blank
1 = LP and FPSCLK disabled during vertical blank

Bit 5 SCS - Shift Clock Stop (STN panels only)
0 = FPSCLK enabled during the first line of vertical blanking
1 = FPSCLK disabled during the first line of vertical blanking

This bit is valid only if SR3D_4 = 0.

Bit 6 FPDS - Flat Panel Data Drive Strength
0 = Drive strength is 6 mA
1 = Drive strength is 12 mA

This bit affects FPD[23:0], PFDE and FPPOL. FPSCLK drive strength is controlled by SR3D_7. This bit must be = 0 for 36-bit XGA panels.

Bit 7 SCDS- Shift Clock Drive Strength
0 = FPSCLK drive strength is 6 mA
1 = FPSCLK drive strength is 12 mA

Flat Panel PWM1 Duty Cycle Register (SR3E)

Read/Write Address: 3C5H, Index 3EH
Power-On Default: 00H

7	6	5	4	3	2	1	0
PWM1 DUTY CYCLE							

Bits 7-0 PWM1 DUTY CYCLE

Value = 256 (x/p)

where x = high time of the PWM1 signal and p = period of the PWM1 signal, both in nanoseconds. The period is determined as explained for SR52_6-4. A programmed value of 00H causes the PWM1 signal to be DC low. A programmed value of FFH causes the PWM1 signal to be DC high.

Flat Panel FRC Tuning 3 Register (SR3F)

Read/Write Address: 3C5H, Index 3FH
Power-On Default: 00H

7	6	5	4	3	2	1	0
TUNING DATA							

The actual value will be supplied by S3 for specific panels.

Flat Panel Pin Configuration Register (SR40)

Read/Write Address: 3C5H, Index 40H
Power-On Default: 00H

7	6	5	4	3	2	1	0
POL	SCS	SCM	FPOFF	FPSCLK DELAY			R

Bit 0 Reserved

Bit 3-1 FPSCLK DELAY

Value = number of nanoseconds to delay FPSCLK

Bit 4 FPOFF - Flat Panel Data and Control Signals Low
0 = Normal operation for flat panel outputs
1 = Force all flat panel data and control signals to logic 0

Bit 5 SCM - Shift Clock Mask
0 = Allow the shift clock (FPSCLK) output to toggle during the non-display interval
1 = Force the shift clock (FPSCLK) output low during the non-display interval

The proper setting of this bit is panel-specific.

Bit 6 SCS - Shift Clock Select (TFT only)
0 = Pixels are clocked on the falling edge of FPSCLK
1 = Pixels are clocked on both the rising and falling edge of FPSCLK

Not all TFT panels provide the double-edge clocking mode.

Bit 7 POL - Polarity Enable (TFT only)
0 = FPPOL pin output disabled
1 = FPPOL pin output enabled

Polarity is available for 18- and 24-bit 1 pixel/clock modes and 2x18-bit 2 pixels/clock mode.

Flat Panel Power Sequence Control Register (SR41)

Read/Write Address: 3C5H, Index 41H
Power-On Default: 00H

7	6	5	4	3	2	1	0
STR		R	R	PUP	PDWN	R	R

Bits 1-0 Reserved

Bit 2 PDWN - Power Down Phase
0 = FPVEE low to FP signals inactive and FP signals inactive to FPVDD low = 32 ms
1 = FPVEE low to FP signals inactive and FP signals inactive to FPVDD low = 128 ms

Bit 3 PUP - Power Up Phase
0 = FPVDD high to FP signals active and FP signals active to FPVEE high = 32 ms
1 = FPVDD high to FP signals active and FP signals active to FPVEE high = 128 ms

Bits 5-4 Reserved

Bits 7-6 STR - Standby Timer Resolution
00 = Reserved
01 = 1 second
10 = Reserved
11 = 64 ms

This resolution applies to the timeout value programmed in SR43_5-0.

Flat Panel Power Management Control Register (SR42)

Read/Write Address: 3C5H, Index 42H
Power-On Default: 00H

7	6	5	4	3	2	1	0
SDB TIMER		SSTB	HSTB	R	R	SSUS	SO

Bit 0 SO - Sync Outputs
0 = If SRD_5-4 = 00b, CLK32 is output on HSYNC during Standby and Suspend;
If SRD_7-6 = 00b, CLK32 is output on VSYNC during Standby and Suspend.
1 = If SRD_5-4 = 00b, normal HSYNC is output during Standby and Suspend;
If SRD_7-6 = 00b, normal VSYNC is output during Standby and Suspend.

If SRD_5-4 is set to something other than 00b, the HSYNC output is determined by this setting (display power management being used).
If SRD_7-6 is set to something other than 00b, the VSYNC output is determined by this setting (display power management being used).

Bit 1 SSUS - Software Suspend
0 = Software suspend disabled
1 = Software suspend enabled

Bits 3-2 Reserved

Bit 4 HSTB - Hardware Standby
0 = Hardware standby disabled
1 = Hardware standby enabled

Bit 5 SSTB - Software Standby
0 = Software standby disabled
1 = Software standby enabled

The BIOS must set this bit to 1 after a power-on reset, program the desired mode and then clear this bit to 0 to initiate a power-up sequence.

Bits 7-6 SDB TIMER - Suspend Debounce Timer
00 = 62.5 µs
01 = 2 seconds
1x = Immediate (used for testing)

Flat Panel Standby Control Register (SR43)

Read/Write Address: 3C5H, Index 43H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	ACT	STANDBY TIMEOUT VALUE					

Bits 5-0 STANDBY TIMEOUT VALUE

Value = number of units to count before Standby mode is entered

The type of unit is selected via bits 7-6 of SR41.

Note: The BIOS must program this field to a non-zero value on power-up and the value must never be programmed to all 0's.

Bit 6 ACT - Activity Enable
0 = Normal standby mode
1 = Activity function enabled

Bit 7 Reserved

Flat Panel Power Management Register (SR44)

Read/Write Address: 3C5H, Index 44H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	STBP	R=0	R=0	R=0	R=0

Bits 3-0 Reserved = 0000b

Bit 4 STBP - Standby Pin
0 = To cause entry to Standby, the STANDBY pin must go high (which starts the Standby counter) and remain high until the idle power down state is reached after the Standby counter expires. Standby is exited when the STANDBY pin goes low. Hardware Standby must be enabled (SR42_4 = 1)
1 = The Standby counter begins counting when hardware Standby is enabled (SR42_4 = 1). Each rising edge of the STANDBY pin resets the counter (if not in Standby) or takes the system out of Standby. When the system reaches the idle power up state after exiting Standby, the Standby counter begins recounting.

Bits 7-5 Reserved

Flat Panel PLL Power Management Register (SR45)

Read/Write Address: 3C5H, Index 45H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	PLL WAIT	

Bits 1-0 PLL WAIT
00 = 2 ms
01 = 4 ms
10 = 8 ms
11 = 16 ms

This is the time from entering Suspend to powering-down of the PLLs and from leaving Suspend to powering-up of the PLLs.

Bits 7-2 Reserved

Flat Panel Power Management Status Register (SR46)

Read Only Address: 3C5H, Index 46H
Power-On Default: 00H

7	6	5	4	3	2	1	0
IDPUP	IDPDN	STBS	R	R	R	R	R

Bits 4-0 Reserved

Bit 5 STBS - Standby Status
0 = Not in Standby mode
1 = In Standby mode

Bit 6 IDPDN - Idle Power Down State
0 = Not in idle power down state
1 = In idle power down state

This is the state immediately after a panel power down sequence.

Bit 7 IDPUP - Idle Power Up State
0 = Not in idle power up state
1 = In idle power up state

This is the state immediately after a panel power up sequence.

CLUT Control Register (SR47)

Read/Write Address: 3C5H, Index 47H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	CLUT SELECT	

Bits 1-0 CLUT SELECT
00 = CLUT1 and CLUT2 enabled for CPU writes. Only CLUT 1 reads are enabled.
01 = CLUT1 only for CPU writes and reads
10 = CLUT2 only for CPU writes and reads
11 = Reserved

CLUT read and write accesses are mapped at 3C7H, 3C8H and 3C9H.

Bits 7-2 Reserved

Icon Mode Register (SR48)

Read/Write Address: 3C5H, Index 48H
Power-On Default: 00H

7	6	5	4	3	2	1	0
ICON ADDRESS LOW				2Y	2X	IMOD	IEN

Bit 0 IEN - Icon Enable
0 = Hardware icon disabled
1 = Hardware icon enabled

Bit 1 IMOD - Icon Mode
0 = 4 opaque colors
1 = 3 opaque colors and 1 transparent color

When this bit is cleared to 0, the color of each icon pixel (2 bits/pixel) is defined as:
00 = Color 0
01 = Color 1
10 = Color 2
11 = Color 3

When this bit is set to 1, the color of each icon pixel (2 bits/pixel) is defined as:
00 = Color 0
01 = Color 1
10 = Color 2
11 = Transparent (the current frame buffer pixel is not overwritten)

The hardware icon colors are defined in SR49.

Bit 2 2X - Double X
0 = Horizontal size is 64 pixels
1 = Horizontal size is 128 pixels

If this bit is set to 1, each pixel is duplicated in the horizontal direction.

Bit 3 2Y - Double Y
0 = Vertical size is 64 pixels
1 = Vertical size is 128 pixels

If this bit is set to 1, each pixel is duplicated in the vertical direction.

Bits 7-4 ICON ADDRESS LOW

Value = Hardware icon address bits 11-8

Bits 19-12 of the address are in SR4E. This is a doubleword address.

Icon Color Stack Register (SR49)

Read/Write Address: 3C5H, Index 49H
Power-On Default: Undefined

This register allows four 24 bits/pixel colors to be defined for the hardware icon. Twelve 8-bit indexed registers are stacked at this address. A read of SR48 resets the index to 0. Each read or write of this register increments the index by 1, so the entire content can be read/written via successive accesses. The colors used for the icon are selected via SR48_1. Colors data for color depths other than 24 bits/pixel use the appropriate number of low-order bits.

7	6	5	4	3	2	1	0
COLOR DATA							

Bits 7-0 COLOR DATA

Index 0 = Color 0 low (blue) byte
Index 1 = Color 0 middle (green) byte
Index 2 = Color 0 high (red) byte
Index 3 = Color 1 low (blue) byte
Index 4 = Color 1 middle (green) byte
Index 5 = Color 1 high (red) byte
Index 6 = Color 2 low (blue) byte
Index 7 = Color 2 middle (green) byte
Index 8 = Color 2 high (red) byte
Index 9 = Color 3 low (blue) byte
Index A = Color 3 middle (green) byte
Index B = Color 3 high (red) byte

The above definition applies when the Streams Processor is enabled or for 24 bpp modes. When the Streams Processor is disabled (CR67_3-2 = 00b), the low order (blue) byte is used as the LUT index for both VGA modes and enhanced 8 bpp modes. Therefore, 4 normally unused locations in the LUT must be programmed with the 4 desired icon colors and the blue color value used to select the appropriate LUT location. For 15/16 bpp modes with the Streams Processor disabled, the appropriate color bits must be programmed into the low order 15 or 16 bits of the color stack each time a 15/16 bpp mode is set.

Icon X Position High Register (SR4A)

Read/Write Address: 3C5H, Index 4AH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	R	R	R	X POSITION HIGH		

Bits 1-0 X POSITION HIGH

Value = High order 3 bits of the icon horizontal coordinate

The low order bits are found in SR4B.

Bits 7-2 Reserved

Icon X Position Low Register (SR4B)

Read/Write Address: 3C5H, Index 4BH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
X POSITION LOW							

Bits 7-0 X POSITION LOW

Value = Low order 8 bits of the icon horizontal coordinate

The high order 3 bits are found in SR4A.

Icon Y Position High Register (SR4C)

Read/Write Address: 3C5H, Index 4CH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	R	R	R	Y POSITION HIGH		

Bits 1-0 Y POSITION HIGH

Value = High order 3 bits of the icon vertical coordinate

The low order bits are found in SR4D.

Bits 7-2 Reserved

Icon Y Position Low Register (SR4D)

Read/Write Address: 3C5H, Index 4DH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
Y POSITION LOW							

Bits 7-0 Y POSITION LOW

Value = Low order 8 bits of the icon vertical coordinate

The high order 3 bits are found in SR4C.

Icon Address High Register (SR4E)

Read/Write Address: 3C5H, Index 4EH
Power-On Default: 00H

7	6	5	4	3	2	1	0
ICON ADDRESS HIGH							

Bits 7-0 ICON ADDRESS HIGH

Value = Hardware icon base address bits 19-12.

Bits 11-8 of the address are in SR48_7-4. This is a doubleword address.

Dual-Scan STN Data Address Register (SR4F)

Read/Write Address: 3C5H, Index 4FH
Power-On Default: 00H

7	6	5	4	3	2	1	0
DD-STN DATA ADDRESS ADJUSTMENT							

Bits 7-0 DD-STN DATA ADDRESS ADJUSTMENT

Value = Number of 8K units to reserve between the top of video memory and the top of the STN data area

The STN data area is by default located at the top of display memory, with its size dependent on the panel resolution. The value in this field specifies how far down the STN data area is pushed to make room for other data such as the hardware icon.

Dual-Scan STN Frame Buffer Size Low Register (SR50)

Read/Write Address: 3C5H, Index 50H
Power-On Default: 00H

7	6	5	4	3	2	1	0
DD-STN FRAME BUFFER SIZE LOW							

Bits 7-0 DD-STN FRAME BUFFER SIZE LOW

Value = lower byte of the STN frame buffer size in quadwords

The STN frame buffer size in quadwords is calculated using the following equation:

Frame Buffer Size = Horizontal size (in quadwords) x 1/2 vertical size (in lines)

Horizontal Size = [(SR61+1) x 3 x 8/64] quadwords rounded up to the nearest integer. Note that the value programmed in SR61 is in 8-pixel characters and data in the frame buffer is 3 bits/pixel. An equivalent formula is:

Horizontal Size = horizontal resolution in pixels x 3/64 (rounded up).

1/2 Vertical Size = 1/2 [SR69 + 1] or:

1/2 Vertical Size = 1/2 vertical resolution in lines

Dual-Scan STN Frame Buffer Size High Register (SR51)

Read/Write Address: 3C5H, Index 51H
Power-On Default: 00H

7	6	5	4	3	2	1	0
DD-STN FRAME BUFFER SIZE HIGH							

Bits 7-0 DD-STN FRAME BUFFER SIZE HIGH

Value = upper byte of STN frame buffer size in quadwords

See SR50 for an explanation of how to determine the value to be programmed in this register.

Flat Panel PWM Register (SR52)

Read/Write Address: 3C5H, Index 52H
Power-On Default: 00H

7	6	5	4	3	2	1	0
PWM1	PWM CLOCK DIVIDE			R	R	PSC	PWM0

Bit 0 PWM0 - PWM0 Enable
0 = PWM0 disabled
1 = PWM0 enabled

Bit 1 PSC - PWM Source Clock Select
0 = Generate PWM signal from the reference clock (XIN input)
1 = Generate PWM signal from the PCI clock (SCLK)

This bit affects generation of both PWM0 and PWM1.

Bits 3-2 Reserved

Bits 6-4 PWM CLOCK DIVIDE
000 = PWM source clock is not pre-divided
001 = PWM source clock is pre-divided by 1.5
010 = PWM source clock is pre-divided by 2
100 = PWM source clock is pre-divided by 3

All other values are reserved.

PWM clock frequency = PWM source clock/pre-divisor/256

The inversion of this is the PWM period used in the PWM0 and PWM1 duty cycle specifications in SR53 and SR3E respectively.

Bit 7 PWM1 - PWM1 Enable
0 = ODD function enabled for input on multiplexed pin
1 = PWM1 function enabled for output on multiplexed pin

Flat Panel PWM0 Duty Cycle Register (SR53)

Read/Write Address: 3C5H, Index 53H
Power-On Default: 00H

7	6	5	4	3	2	1	0
PWM0 DUTY CYCLE							

Bits 7-0 PWM0 DUTY CYCLE

Value = 256 (x/p)

where x = high time of the PWM0 signal and p = period of the PWM0 signal, both in nanoseconds. The period is determined as explained for SR52_6-4. A programmed value of 00H causes the PWM0 signal to be DC low. A programmed value of FFH causes the PWM0 signal to be DC high.

Flat Panel Horizontal Compensation 1 Register (SR54)

Read/Write Address: 3C5H, Index 54H
Power-On Default: 00H

7	6	5	4	3	2	1	0
FPLG	HEFE		HCE	GRAPH EXP		TEXT EXP	

Bits 1-0 TEXT EXP - Text Mode Horizontal Expansion
00 = Horizontal expansion disabled
01 = Horizontal expansion enabled up to a maximum expansion factor of 1.25
10 = Reserved
11 = Horizontal expansion enabled up to the horizontal panel size. For VGA panels, 9-dot text modes will be forced to 8-dot text modes.

The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 800 columns to limit the expansion and eliminate the undesirable visual effects.

Bits 3-2 GRAPH EXP - Graphics Mode Horizontal Expansion
00 = Horizontal expansion disabled
01 = Horizontal expansion enabled up to a maximum expansion factor of 1.25
10 = Reserved
11 = Horizontal expansion enabled up to the horizontal panel size. For VGA panels, 9-dot text modes will be forced to 8-dot text modes.

The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 800 columns to limit the expansion and eliminate the undesirable visual effects.

Bit 4 HCE - Horizontal Centering Enable
0 = Horizontal centering disabled
1 = Horizontal centering enabled

Bits 6-5 HEFE - Horizontal Expansion Filter Enable
00 = Horizontal expansion filter disabled
01 = Horizontal expansion filter enabled in flat panel mode
10 = Reserved
11 = Reserved

The horizontal expansion filter is used to smooth the effect of horizontal expansion.

Bit 7 FPLG - Flat Panel Line Graphics Enable
0 = The ninth dot of a text character (SR1_0 = 0) is the same color as the background
1 = Special line graphics character codes enabled

This bit performs the same function as AR10_2 in CRT mode.

Flat Panel Horizontal Compensation 2 Register (SR55)

Read/Write Address: 3C5H, Index 55H
Power-On Default: 00H

The bits in this register control enabling of horizontal expansion in specific text/graphics modes. They are effective only if text mode horizontal expansion is enabled via SR54_1-0. Horizontal expansion for all other modes not controlled by these bits is controlled by SR54_3-0.

7	6	5	4	3	2	1	0
ATHE	R	R	1024C	800C	640C	80C	40C

Bit 0 40C - 40-character Text Mode Horizontal Expansion Enable
0 = Horizontal expansion disabled in 40-character text mode
1 = Horizontal expansion enabled in 40-character text mode

This bit is effective only if text mode horizontal expansion is enabled via SR54_1-0.

Bit 1 80C - 80-character Text Mode Horizontal Expansion Enable
0 = Horizontal expansion disabled in 80-character text mode
1 = Horizontal expansion enabled in 80-character text mode

This bit is effective only if text mode horizontal expansion is enabled via SR54_1-0.

Bit 2 640C - 320/640-column Graphics Mode Horizontal Expansion Enable
0 = Horizontal expansion disabled in 320/640-column graphics mode
1 = Horizontal expansion enabled in 320/640-column graphics mode

This bit is effective only if graphics mode horizontal expansion is enabled via SR54_3-2.

Bit 3 800C - 800-column Graphics Mode Horizontal Expansion Enable
0 = Horizontal expansion disabled in 800-column graphics mode
1 = Horizontal expansion enabled in 800-column graphics mode

This bit is effective only if graphics mode horizontal expansion is enabled via SR54_3-2.

Bit 4 1024C - 1024-column Graphics Mode Horizontal Expansion Enable
0 = Horizontal expansion disabled in 1024-column graphics mode
1 = Horizontal expansion enabled in 1024-column graphics mode

This bit is effective only if graphics mode horizontal expansion is enabled via SR54_3-2.

Bits 6-5 Reserved

Bit 7 ATHE - Alternate Text Mode Horizontal Expansion
0 = Standard text mode horizontal expansion
1 = Alternate text mode horizontal expansion

This bit affects text mode expansion for 800-column or 1024-column panels.

Flat Panel Vertical Compensation 1 Register (SR56)

Read/Write Address: 3C5H, Index 56H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	VCE	GRAPH EXP		TEXT EXP	

Bits 1-0 TEXT EXP - Text Mode Vertical Expansion
00 = Vertical expansion disabled
01 = Vertical expansion enabled up to a maximum of 480 lines
10 = Reserved
11 = Vertical expansion enabled up to the vertical panel size

The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 480 lines to limit the expansion and eliminate the undesirable visual effects.

Bits 3-2 GRAPH EXP - Graphics Mode Vertical Expansion
00 = Vertical expansion disabled
01 = Vertical expansion enabled up to a maximum of 480 lines
10 = Reserved
11 = Vertical expansion enabled up to the vertical panel size.

The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 480 lines to limit the expansion and eliminate the undesirable visual effects.

Bit 4 VCE - Vertical Centering Enable
0 = Vertical centering disabled
1 = Vertical centering enabled

This bit is effective only if vertical expansion is enabled via bits 3-2 of this register.

Bits 7-5 Reserved

Flat Panel Vertical Compensation 2 Register (SR57)

Read/Write Address: 3C5H, Index 57H
Power-On Default: 00H

This register is used only when flat panel operation is enabled (SR31_4 = 1). The bits in this register control enabling of vertical expansion in specific text/graphics modes. Vertical expansion for all other modes not controlled by these bits is controlled by SR56_3-0.

7	6	5	4	3	2	1	0
ATVE	768G	600G	480G	200G	350G	200T	350T

Bit 0 350T - 350-line Text Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 350-line text mode
1 = Vertical expansion enabled in 350-line text mode

This bit is effective only if text mode vertical expansion is enabled via SR56_0 = 1 or SR56_1 = 1.

Bit 1 200T - 200/400-line Text Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 200/400-line text mode
1 = Vertical expansion enabled in 200/400-line text mode

This bit is effective only if text mode vertical expansion is enabled via SR56_0 = 1 or SR56_1 = 1.

Bit 2 350G - 350-line Graphics Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 350-line graphics mode
1 = Vertical expansion enabled in 350-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56_2 = 1 or SR56_3 = 1.

Bit 3 200G - 200/400-line Graphics Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 200/400-line graphics mode
1 = Vertical expansion enabled in 200/400-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56_2 = 1 or SR56_3 = 1.

Bit 4 480G - 480-line Graphics Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 480-line graphics mode
1 = Vertical expansion enabled in 480-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56_2 = 1 or SR56_3 = 1.

Bit 5 600G - 600-line Graphics Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 600-line graphics mode
1 = Vertical expansion enabled in 600-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56_2 = 1 or SR56_3 = 1.

Bit 6 768G - 768-line Graphics Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 768-line graphics mode
1 = Vertical expansion enabled in 768-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56_2 = 1 or SR56_3 = 1.

Bit 7 ATVE - Alternate Text Mode Vertical Expansion
0 = Standard text mode vertical expansion
1 = Alternate text mode vertical expansion

This bit affects text mode expansion for 200/400-line text modes for 600-line or 768-line panels.

Flat Panel Horizontal Border Register (SR58)

Read Only Address: 3C5H, Index 58H
Power-On Default: 00H

7	6	5	4	3	2	1	0
FP HORIZONTAL BORDER 7-0							

Bits 7-0 FP HORIZONTAL BORDER 7-0

9-bit Value = number of character clocks per horizontal line not used by the video image.

Bit 8 of this value is in SR59_0.

Flat Panel Horizontal Expansion Factor Register (SR59)

Read Only Address: 3C5H, Index 59H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	HORIZ EXP FACTOR			R	R	R	HB8

Bit 0 HB8 - Flat Panel Horizontal Border Bit 8

Bits 7-0 are in SR58.

Bits 3-1 Reserved

Bits 6-4 HORIZ EXP FACTOR
000 = panel size < image size
001 = 1 1/8x image size > panel size ≥ image size
010 = illegal
011 = 1 1/4x image size > panel size ≥ 1 1/8x image size
100 = 1 1/2x image size > panel size ≥ 1 1/4x image size
101 = illegal
110 = 2x image size > panel size ≥ 1 1/2x image size
111 = panel size ≥ 2x image size

Bit 7 Reserved

Flat Panel Vertical Border Register (SR5A)

Read Only Address: 3C5H, Index 5AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
FP VERTICAL BORDER 7-0							

Bits 7-0 FP VERTICAL BORDER 7-0

9-bit Value = number of lines not used by the video image

Bit 8 of this value is SR5B_0.

Flat Panel Vertical Expansion Factor Register (SR5B)

Read Only Address: 3C5H, Index 5BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
VERT EXP FACTOR				LRI	VCD	VED	VB8

Bit 0 VB8 - Flat Panel Vertical Border Bit 8

Bits 7-0 are in SR5A.

Bit 1 VED - Vertical Expansion Detect
0 = No vertical expansion
1 = Automatic vertical expansion is being done or would be being done if enabled.

This bit is used only for test purposes.

Bit 2 VCD - Vertical Centering Detect
0 = No vertical centering
1 = Automatic vertical centering is being done (it must be enabled)

This bit is used only for test purposes.

Bit 3 LRI - Line Repeat Indicator
0 = Current scan line will be repeated on the next scan line
1 = Current scan line will not be repeated on on the next scan line

This bit is used only for test purposes.

Bits 7-4 VERT EXP FACTOR
0000 = No expansion
0001 = Illegal
0010 = Double every third line
0011 = Expand 16-line text to 19-line text
0100 = Double every fifth line
0101 = Expand 14-line text to 19-line text
0110 = Double every fourth line
0111 = Double every second line
1000 = Double every line
1001 = Double three lines and triple the fourth, repeat
1010 = Expand 8-line text to 19-line text
1011 = Double four lines and triple the fifth, repeat
1100 = Double two lines and triple the third, repeat
1101 = Illegal
1110 = Double one line and triple the second, repeat
1111 = Quadruple every line

Flat Panel Display Enable Position Control Register (SR5C)

Read/Write Address: 3C5H, Index 5CH
Power-On Default: Undefined

The fields in this register are effective only for Enhanced modes (8 bits/pixel or higher). The BIOS should program this register to 77H on reset.

7	6	5	4	3	2	1	0
FPDEC2				FPDEC1			

Bits 3-0 FPDEC1 - Flat Panel Display Enable Control 1

value = starting position of the horizontal and vertical display enables for Controller 1

This field should normally be left at its default value of 0111b. A smaller value causes the display enables to be moved earlier by the difference between the programmed value and the nominal value. A larger value causes the display enables to be moved later by the difference between the programmed value and the nominal value. Each difference unit causes a shift of 1 DCLK.

Bits 7-4 FPDEC2 - Flat Panel Display Enable Control 2

value = starting position of the horizontal and vertical display enables for Controller 2

This field should normally be left at its default value of 0111b. A smaller value causes the display enables to be moved earlier by the difference between the programmed value and the nominal value. A larger value causes the display enables to be moved later by the difference between the programmed value and the nominal value. Each difference unit causes a shift of 1 DCLK.

Flat Panel/CRT Sync Position Control Register (SR5D)

Read/Write Address: 3C5H, Index 5DH
Power-On Default: 77H

The fields in this register are effective only for Enhanced modes (8 bits/pixel or higher). The BIOS should program this register to 77H on reset.

7	6	5	4	3	2	1	0
FP/CRTSC2				FP/CRTSC1			

Bits 3-0 FP/CRTSC1 - Flat Panel/CRT Sync Control 1

value = starting position of the horizontal and vertical syncs for Controller 1

This field should normally be left at its default value of 0111b. A smaller value causes the syncs to be moved earlier by the difference between the programmed value and the nominal value. A larger value causes the syncs to be moved later by the difference between the programmed value and the nominal value. Each difference unit causes a shift of 1 DCLK.

Bits 7-4 FP/CRTSC2 - Flat Panel/CRT Sync Control 2

value = starting position of the horizontal and vertical display enables for Controller 2

This field should normally be left at its default value of 0111b. A smaller value causes the syncs to be moved earlier by the difference between the programmed value and the nominal value. A larger value causes the syncs to be moved later by the difference between the programmed value and the nominal value. Each difference unit causes a shift of 1 DCLK.

Flat Panel BIOS Scratch 1 Register (SR5E)

Read/Write Address: 3C5H, Index 5EH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
RESERVED FOR BIOS							

Bits 7-0 RESERVED FOR BIOS

Flat Panel BIOS Scratch 2 Register (SR5F)

Read/Write Address: 3C5H, Index 5FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
RESERVED FOR BIOS							

Bits 7-0 RESERVED FOR BIOS

Flat Panel Horizontal Total Register (SR60)

Read/Write Address: 3C5H, Index 60H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL TOTAL 7-0							

Bits 7-0 FP HORIZONTAL TOTAL 7-0

9-bit Value = [number of character clocks in one scan line] - 5

A character clock is always 8 FPSCLKs (FP dot clocks). The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66_0.

Flat Panel Horizontal Panel Size Register (SR61)

Read/Write Address: 3C5H, Index 61H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL PANEL SIZE 7-0							

Bits 7-0 FP HORIZONTAL PANEL SIZE 7-0

9-bit Value = [horizontal panel resolution in character clocks] - 1

A character clock is always 8 FPSCLKs (FP dot clocks). For example, for a VGA panel with a horizontal resolution of 640, the programmed value would be the binary equivalent of [640/8] - 1. The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66_1.

Flat Panel Horizontal Blank Start Register (SR62)

Read/Write Address: 3C5H, Index 62H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL BLANK START 7-0							

Bits 7-0 FP HORIZONTAL BLANK START 7-0

9-bit Value = character clock counter value at which blanking begins

A character clock is always 8 FPSCLKs (FP dot clocks). The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66_2.

Flat Panel Horizontal Blank End Register (SR63)

Read/Write Address: 3C5H, Index 63H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	R	FP HORIZONTAL BLANK END 4-0				

Bits 4-0 FP HORIZONTAL BLANK END 4-0

6-bit Value = least significant 6 bits of the character clock counter value at which blanking ends

A character clock is always 8 FPSCLKs (FP dot clocks). To obtain this value, add the desired width of the vertical blanking pulse in character clocks to the value in the FP Horizontal Blank Start register, also in character clocks. The 5 least significant bits of this value are programmed into this field. The programmed value is independent of horizontal compensation and applies to all modes. Bit 5 of this value is SR65_7. If the horizontal blank period is more than 64 character clocks, then SR66_3 must be set to 1.

Bits 7-5 Reserved

Flat Panel Horizontal Sync Start Register (SR64)

Read/Write Address: 3C5H, Index 64H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL SYNC START 7-0							

Bits 7-0 FP HORIZONTAL SYNC START 7-0

8-bit Value = character clock counter value at which the horizontal sync pulse (LP) becomes active

A character clock is always 8 FPSCLKs (FP dot clocks). The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66_4.

Flat Panel Horizontal Sync End Register (SR65)

Read/Write Address: 3C5H, Index 65H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
BE5	R	R	FP HORIZONTAL SYNC END 4-0				

Bits 4-0 FP HORIZONTAL SYNC END 4-0

5-bit Value = least significant 5 bits of the character clock counter value at which the horizontal sync pulse (LP) becomes inactive

A character clock is always 8 FPSCLKs (FP dot clocks). To obtain this value, add the desired width of the horizontal sync pulse in character clocks to the value in the FP Horizontal Sync Start register. The 5 least significant bits of this value are programmed into this field. The programmed value is independent of horizontal compensation and applies to all modes. If the horizontal sync period is more than 32 character clocks, SR66_5 must be set to 1.

Bits 6-5 Reserved

Bit 7 BE5 - FP Horizontal Sync End Bit 5

Bits 4-0 are in this register.

Flat Panel Horizontal Overflow Register (SR66)

Read/Write Address: 3C5H, Index 66H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HSE5	HSS8	HBP	HBS8	HPS8	HT8

Bit 0 FP Horizontal Total Bit 8

Bits 7-0 are in SR60.

Bit 1 FP Horizontal Panel Size Bit 8

Bits 7-0 are in SR61.

Bit 2 FP Horizontal Blank Start Bit 8

Bits 7-0 are in SR62.

Bit 3 FP Horizontal Blank Period
0 = Flat panel horizontal blank period is 64 character clocks or less
1 = Flat panel horizontal blank period is greater than 64 character clocks

See SR 63_4-0.

Bit 4 FP Horizontal Sync Start Bit 8

Bits 7-0 are in SR64.

Bit 5 FP Horizontal Sync Period
0 = Flat panel horizontal sync period is 32 character clocks or less
1 = Flat panel horizontal sync period is greater than 32 character clocks

See SR65_4-0.

Bits 7-6 Reserved

Flat Panel Vertical Total Register (SR68)

Read/Write Address: 3C5H, Index 68H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL TOTAL 7-0							

Bits 7-0 FP VERTICAL TOTAL 7-0

11-bit Value = [number of scan lines from one vertical sync pulse (FLM) active to the next vertical sync pulse active] - 2

The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6E_2-0.

Flat Panel Vertical Panel Size Register (SR69)

Read/Write Address: 3C5H, Index 69H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL PANEL SIZE 7-0							

Bits 7-0 FP VERTICAL PANEL SIZE 7-0

11-bit Value = [vertical panel resolution in scan lines] - 1

For example, for a VGA panel with a vertical resolution of 480, the programmed value would be the binary equivalent of 480 - 1. The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6E_6-4.

Flat Panel Vertical Blank Start Register (SR6A)

Read/Write Address: 3C5H, Index 6AH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL BLANK START 7-0							

Bits 7-0 FP VERTICAL BLANK START 7-0

11-bit Value = scan line counter value at which blanking begins

The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6F_2-0.

Flat Panel Vertical Blank End Register (SR6B)

Read/Write Address: 3C5H, Index 6BH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL BLANK END 7-0							

Bits 7-0 FP VERTICAL BLANK END 7-0

Value = least significant 8 bits of the scan line counter value at which blanking ends

To obtain this value, add the desired width of the vertical blanking pulse in scan lines to the value in the FP Vertical Blank Start register, also in scan lines. The 8 least significant bits of this value are programmed into this field. The programmed value is independent of vertical compensation and applies to all modes.

Flat Panel Vertical Sync Start Register (SR6C)

Read/Write Address: 3C5H, Index 6CH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL SYNC START 7-0							

Bits 7-0 FP VERTICAL SYNC START 7-0

11-bit Value = [scan line counter value at which the vertical sync pulse (FLM) becomes active] -1

The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6F_6-4.

Flat Panel Vertical Sync End Register (SR6D)

Read/Write Address: 3C5H, Index 6DH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	R	R	FP VERTICAL SYNC END 3-0			

Bits 3-0 FP VERTICAL SYNC END 3-0

4-bit Value = least significant 4 bits of the character clock counter value at which the vertical sync pulse (FLM) becomes inactive

To obtain this value, add the desired width of the vertical sync pulse in scan lines to the value in the FP Vertical Sync Start register, also in scan lines. The 4 least significant bits of this value are programmed into this field. The programmed value is independent of vertical compensation and applies to all modes.

Bits 7-4 Reserved

Flat Panel Vertical Overflow 1 Register (SR6E)

Read/Write Address: 3C5H, Index 6EH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	VPS10-8			R	VT10-8		

Bits 2-0 VT10-8 - FP Vertical Total Bits 10-8

Bits 7-0 are in SR68.

Bit 3 Reserved

Bits 6-4 VPS10-8 - FP Vertical Panel Size Bits 10-8

Bits 7-0 are in SR69.

Bit 7 Reserved

Flat Panel Vertical Overflow 2 Register (SR6F)

Read/Write Address: 3C5H, Index 6FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	VSS10-8			R	VBS10-8		

Bits 2-0 VBS10-8 - FP Vertical Blank Start Bits 10-8

Bits 7-0 are in SR6A.

Bit 3 Reserved

Bits 6-4 VSS10-8 - FP Vertical Sync Start Bits 10-8

Bits 7-0 are in SR6C.

Bit 7 Reserved

Appendix A: Listing of Raster Operations

M5 supports all 256 triadic raster operations (ROPs) for BitBLTs as defined by Microsoft for Windows. The coding for these is found on the following pages.

The HEX value in the first column is the ROP code. This value must be programmed into bits 7-0 of D2E8H at the time that a ROPBLT command is executed.

The effect of the ROP is shown in reverse Polish notation in the second column. This is interpreted as follows:

S = Source bitmap

P = Pattern

D = Destination bitmap

The source bitmap can be either the CPU or the current screen, as specified by bit 7 of the Command Set register. A CPU source can be either monochrome or color, as specified by bit 6 of the Command Set register. A screen source is always color.

The pattern may be either monochrome or color, as specified by bit 8 of the Command Set register.

The destination bitmap is always the screen. It is always color (as opposed to monochrome).

The boolean operators used as as follows:

o = bitwise OR

x = bitwise EXCLUSIVE OR

a = bitwise AND

n = bitwise NOT (inverse)

For example, ROP 16H is PSDPSanaxx. The pattern is first ANDed with the source [PSD(PaS)naxx]. The result is inverted and then ANDed with the destination [PS((Da(notPaS))xx. This result is EXCLUSIVE ORed with the source. Finally, the result of this is EXCLUSIVE ORed with the pattern.

Programming using ROPBLTs is explained in Enhanced Programming section.

HEX	In Reverse Polish
00	0
01	DPSoon
02	DPSona
03	PSon
04	SDPona
05	DPon
06	PDSxnon
07	PDSaon
08	SDPnaa
09	PDSxon
0A	DPna
0B	PSDnaon
0C	SPna
0D	PDSnaon
0E	PDSonon
0F	Pn
10	PDSona
11	DSon
12	SDPxnon
13	SDPaon
14	DPSxnon
15	DPSaon
16	PSDPSanaxx
17	SSPxDSxaxn
18	SPxPDxa
19	SDPSanaxn
1A	PDSPaox
1B	SDPSxaxn
1C	PSDPaox
1D	DSPDxaxn
1E	PDSox
1F	PDSoan
20	DPSnaa
21	SDPxon
22	DSna
23	SPDnaon
24	SPxDSxa
25	PDSPanaxn
26	SDPSaox
27	SDPSxnox
28	DPSxa
29	PSDPSaoxxn
2A	DPSana
2B	SSPxPDxaxn

HEX	In Reverse Polish
2C	SPDSoax
2D	PSDnox
2E	PSDPxox
2F	PSDnoan
30	PSna
31	SDPnaon
32	SDPSoox
33	Sn
34	SPDSaox
35	SPDSxnox
36	SDPox
37	SDPoan
38	PSDPoax
39	SPDnox
3A	SPDSxox
3B	SPDnoan
3C	PSx
3D	SPDSonox
3E	SPDSnaox
3F	PSan
40	PSDnaa
41	DPSxon
42	SDxPDxa
43	SPDSanaxn
44	SDna
45	DPSnaon
46	DSPDaox
47	PSDPxaxn
48	SDPxa
49	PDSPDaoxxn
4A	DPSDoax
4B	PDSnox
4C	SDPana
4D	SSPxDSxoxn
4E	PDSPxox
4F	PDSnoan
50	PDna
51	DSPnaon
52	DPSDaox
53	SPDSxaxn
54	DPSonon
55	Dn
56	DPSox
57	DPSoan

HEX	In Reverse Polish
58	PDSPoax
59	DPSnox
5A	DPx
5B	DPSDonox
5C	DPSDxox
5D	DPSnoan
5E	DPSDnaox
5F	DPan
60	PDSxa
61	DSPDSaoxxn
62	DSPDoax
63	SDPnox
64	SDPSoax
65	DSPnox
66	DSx
67	SDPSonox
68	DSPDSonoxxn
69	PDSxxn
6A	DPSax
6B	PSDPSoaxxn
6C	SDPax
6D	PDSPDoaxxn
6E	SDPSnoax
6F	PDSxnan
70	PDSana
71	SSDxPDxaxn
72	SDPSxox
73	SDPnoan
74	DSPDxox
75	DSPnoan
76	SDPSnaox
77	DSan
78	PDSax
79	DSPDSoaxxn
7A	DPSDnoax
7B	SDPxnan
7C	SPDSnoax
7D	DPSxnan
7E	SPxDSxo
7F	DPSaan
80	DPSaa
81	SPxDSxon
82	DPSxna
83	SPDSnoaxn

HEX	In Reverse Polish
84	SDPxna
85	PDSPnoaxn
86	DSPDSoaxx
87	PDSaxn
88	DSa
89	SDPSnaoxn
8A	DSPnoa
8B	DSPDxoxn
8C	SDPnoa
8D	SDPSxoxn
8E	SSDxPDxax
8F	PDSanan
90	PDSxna
91	SDPSnoaxn
92	DPSDPoaxx
93	SPDaxn
94	PSDPSoaxx
95	DPSaxn
96	DPSxx
97	PSDPSonoxx
98	SDPSonoxn
99	DSxn
9A	DPSnax
9B	SDPSoaxn
9C	SPDnax
9D	DSPDoaxn
9E	DSPDSaoxx
9F	PDSxan
A0	DPa
A1	PDSPnaoxn
A2	DPSnoa
A3	DPSDxoxn
A4	PDSPonoxn
A5	PDxn
A6	DSPnax
A7	PDSPoaxn
A8	DPSoa
A9	DPSoxn
AA	D
AB	DPSono
AC	SPDSxax
AD	DPSDaoxn
AE	DSPnao
AF	DPno

HEX	In Reverse Polish
B0	PDSnoa
B1	PDSPxoxn
B2	SSPxDSxox
B3	SDPanan
B4	PSDnax
B5	DPSDoaxn
B6	DPSDPaoxx
B7	SDPxan
B8	PSDPxax
B9	DSPDaoxn
BA	DPSnao
BB	DSno
BC	SPDSanax
BD	SDxPDxan
BE	DPSxo
BF	DPSano
C0	PSa
C1	SPDSnaoxn
C2	SPDSonoxn
C3	PSxn
C4	SPDnoa
C5	SPDSxoxn
C6	SDPnax
C7	PSDPoaxn
C8	SDPoa
C9	SPDoxn
CA	DPSDxax
CB	SPDSaoxn
CC	S
CD	SDPono
CE	SDPnao
CF	SPno
D0	PSDnoa
D1	PSDPxoxn
D2	PDSnax
D3	SPDSoaxn
D4	SSPxPDxax
D5	DPSanan
D6	PSDPSaoxx
D7	DPSxan
D8	PDSPxax
D9	SDPSaoxn
DA	DPSDanax
DB	SPxDSxan

HEX	In Reverse Polish
DC	SPDnao
DD	SDno
DE	SDPxo
DF	SDPano
E0	PDSoa
E1	PDSoxn
E2	DSPDxax
E3	PSDPaoxn
E4	SDPSxax
E5	PDSPaoxn
E6	SDPSanax
E7	SPxPDxan
E8	SSPxDSxax
E9	DSPDSanaxxn
EA	DPSao
EB	DPSxno
EC	SDPao
ED	SDPxno
EE	DSo
EF	SDPnoo
F0	P
F1	PDSono
F2	PDSnao
F3	PSno
F4	PSDnao
F5	PDno
F6	PDSxo
F7	PDSano
F8	PDSao
F9	PDSxno
FA	DPo
FB	DPSnoo
FC	PSo
FD	PSDnoo
FE	DPSoo
FF	1

Appendix B: Register Reference

This Appendix contains tables listing all the registers in each of categories corresponding to Sections 16-26 of this data book.

- VGA
- Extended Sequencer
- Extended CRTC
- S3d
- Streams Processor
- DMA
- Miscellaneous Control
- LPB
- PCI Configuration Space
- TV
- Flat Panel

Within each table, registers are listed in order of increasing addresses/indices. Name, address, register bit descriptions with read/write status and the page number of the detailed register description are provided for each register. All addresses and indices are hexadecimal values.

B.1 VGA REGISTERS

? = B for monochrome, D for color.

Table B-1. VGA Registers

Address	Index Bit(s)		Register Name Bit Description	Description Page
General or External Registers				
3C2			**Miscellaneous Output**	**16-1**
	0	W	Color emulation. Address based at 3Dx	
	1	W	Enable CPU access of video memory	
	3-2	W	DCLK select	
	4	W	Reserved	
	5	W	Select the high 64K page of memory	
	6	W	Make HSYNC an active low signal	
	7	W	Make VSYNC an active low signal	
	7-6	W	(Alternate) Vertical graphics resolution	
3CC			**Miscellaneous Output**	**16-1**
	0	R	Color emulation. Address based at 3Dx	
	1	R	Enable CPU access of video memory	
	3-2	R	DCLK select	
	4	R	Reserved	
	5	R	Select the high 64K page of memory	
	6	R	Make HSYNC an active low signal	
	7	R	Make VSYNC an active low signal	
	7-6	R	(Alternate) Vertical graphics resolution	
3?A			**Feature Control**	**16-3**
	2-0	W	Reserved	
	3	W	VSYNC is ORed with the internal display enable signal	
	7-4	W	Reserved	
3CA			**Feature Control**	**16-3**
	2-0	R	Reserved	
	3	R	VSYNC is ORed with the internal display enable signal	
	7-4	R	Reserved	
3C2			**Input Status 0**	**16-3**
	3-0	R	Reserved	
	4	R	The internal SENSE signal is a logical 1	
	6-5	R	Reserved	
	7	R	Vertical retrace interrupt to the CPU is pending	

Table B-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?A			**Input Status 1**	**16-4**
	0	R	The display in not in active display mode	
	1	R	Reserved	
	2	R	Reserved =1	
	3	R	Vertical retrace period is active	
	5-4	R	Feedback of two color outputs for test purposes	
	7-6	R	Reserved	
3C3			**Video Subsystem Enable**	**16-4**
	0	W	Enable the chip	
	7-1	R/W	Reserved	
Sequencer Registers				
3C4			**Sequencer Index**	**16-5**
	4-0	R/W	Index to the sequencer register to be accessed	
	7-5	R/W	Reserved	
3C5			**Sequencer Data**	**16-5**
	7-0	R/W	Data to or from the sequencer register accessed	
3C5	**00**		**Reset (SR0)**	**16-6**
	0	R/W	Asynchronous reset (not functional for ViRGE/MX)	
	1	R/W	Synchronous reset (not functional for ViRGE/MX)	
	7-2	R/W	Reserved	
3C5	**01**		**Clocking Mode (SR1)**	**16-6**
	0	R/W	Character clocks are 8 dots wide	
	1	R/W	Reserved	
	2	R/W	Load the video serializers every second character clock	
	3	R/W	The internal character clock is 1/2 the DCLK frequency	
	4	R/W	Load the video serializers every fourth character clock	
	5	R/W	Screen is turned off	
3C5	**02**		**Enable Write Plane (SR2)**	**16-7**
	3-0	R/W	Enables a CPU write to the corresponding color plane	
	7-4	R/W	Reserved	
3C5	**03**		**Character Font Select (SR3)**	**16-8**
	4, 1-0	R/W	Select Font B	
	5,3-2	R/W	Select Font A	
	7-6	R/W	Reserved	

Table B-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**04**		**Memory Mode Control (SR4)**	**16-9**
	0	R/W	Reserved	
	1	R/W	Memory access to 256K allowed (required for VGA)	
	2	R/W	Sequential addressing for CPU video memory accesses	
	3	R/W	Modulo 4 addressing for CPU video memory accesses	
	7-4	R/W	Reserved	
CRT Controller Registers				
3?4			**CRT Controller Index**	**16-10**
	7-0	R/W	Index to the CRTC register to be accessed	
3?5			**CRT Controller Data**	**16-10**
	7-0	R/W	Data to or from the CRTC register accessed	
3?5	**00**		**Horizontal Total (CR0) - Paired**	**16-11**
	7-0	R/W	Number of characters in a line -5	
3?5	**01**		**Horizontal Display End (CR1) - Paired**	**16-11**
	7-0	R/W	One less than the total number of displayed characters	
3?5	**02**		**Start Horizontal Blank (CR2) - Paired**	**16-12**
	7-0	R/W	Character count where horizontal blanking starts	
3?5	**03**		**End Horizontal Blank (CR3) - Paired**	**16-12**
	4-0	R/W	End position of horizontal blanking	
	6-5	R/W	Display enable skew in character clocks	
	7	R/W	Reserved	
3?5	**04**		**Start Horizontal Sync Position (CR4) - Paired**	**16-13**
	7-0	R/W	Character count where HSYNC goes active	
3?5	**05**		**End Horizontal Sync Position (CR5) - Paired**	**16-13**
	4-0	R/W	Position where HSYNC goes inactive	
	6-5	R/W	Horizontal retrace end delay in character clocks	
	7	R/W	End horizontal blanking bit 5	
3?5	**06**		**Vertical Total (CR6) - Paired**	**16-14**
	7-0	R/W	Number of lines - 2	

Table B-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**07**		**CRTC Overflow (CR7) - Paired**	**16-14**
	0	R/W	Vertical total bit 8	
	1	R/W	Vertical display end bit 8	
	2	R/W	Vertical retrace start bit 8	
	3	R/W	Start vertical blank bit 8	
	4	R/W	Line compare bit 8 (not paired)	
	5	R/W	Vertical total bit 9	
	6	R/W	Vertical display end bit 9	
	7	R/W	Vertical retrace start bit 9	
3?5	**08**		**Preset Row Scan (CR8)**	**16-15**
	4-0	R/W	Line where first character row begins	
	6-5	R/W	Number of bytes to pan horizontally - Paired	
	7	R/W	Reserved	
3?5	**09**		**Maximum Scan Line (CR9)**	**16-15**
	4-0	R/W	Character height in scan lines -1	
	5	R/W	Start vertical blank bit 9 - Paired	
	6	R/W	Line compare bit 9	
	7	R/W	Double scanning (repeat each line) enabled - Paired	
3?5	**0A**		**Cursor Start Scan Line (CRA)**	**16-16**
	4-0	R/W	Cursor starting line within the character cell	
	5	R/W	Turns off the cursor	
	7-6	R/W	Reserved	
3?5	**0B**		**Cursor End Scan Line (CRB)**	**16-16**
	4-0	R/W	Cursor ending line within the character cell	
	6-5	R/W	Cursor skew to right in characters	
	7	R/W	Reserved	
3?5	**OC**		**Start Address High (CRC) - Paired**	**16-17**
	7-0	R/W	Bits 15-8 of the display start address	
3?5	**OD**		**Start Address Low (CRD) - Paired**	**16-17**
	7-0	R/W	Bits 7-0 of the display start address	
3?5	**OE**		**Cursor Location Address High (& Hardware Cursor Foreground Color in Enhanced Mode) (CRE)**	**16-18**
	7-0	R/W	Bits 15-8 of the cursor location start address	
3?5	**OF**		**Cursor Location Address Low (& Hardware Cursor Background Color in Enhanced Mode) (CRF)**	**16-18**
	7-0	R/W	Bits 7-0 of the cursor location start address	

Table B-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**10**		**Vertical Retrace Start (CR10 - Paired**	**16-18**
	7-0	R/W	Vertical retrace start in scan lines	
3?5	**11**		**Vertical Retrace End (CR11)**	**16-19**
	3-0	R/W	Vertical retrace end in scan lines - Paired	
	4	R/W	Clear the vertical retrace interrupt flip-flop	
	5	R/W	Disable vertical interrupts	
	6	R/W	Five RAM refresh cycles per horizontal line	
	7	R/W	Lock writes to CR0-CR7 - Paired	
3?5	**12**		**Vertical Display End (CR12)**	**16-20**
	7-0	R/W	Number of scan lines of active video	
3?5	**13**		**Offset (CR13) - Paired**	**16-20**
	7-0	R/W	Memory start address jump from one scan line to the next	
3?5	**14**		**Underline Location (CR14)**	**16-21**
	4-0	R/W	Horizontal scan line where underline occurs	
	5	R/W	Memory address counter increment is 4 character clocks	
	6	R/W	Memory accessed as doublewords	
	7	R/W	Reserved	
3?5	**15**		**Start Vertical Blank (CR15) - Paired**	**16-21**
	7-0	R/W	Horizontal scan line where vertical blanking starts	
3?5	**16**		**End Vertical Blank (CR16) - Paired**	**16-22**
	7-0	R/W	Horizontal scan line where vertical blanking ends	
3?5	**17**		**CRTC Mode Control (CR17)**	**16-22**
	0	R/W	Enable bank 2 mode for CGA emulation	
	1	R/W	Enable bank 4 mode for CGA emulation	
	2	R/W	Use horizontal retrace clock divided by 2 - Paired	
	3	R/W	Enable count by 2 mode	
	4	R/W	Reserved	
	5	R/W	Enable CGA mode address wrap	
	6	R/W	Use byte address mode	
	7	R/W	Horizontal and vertical retrace signals enabled - Paired	
3?5	**18**		**Line Compare (CR18)**	**16-24**
	7-0	R/W	Line at which memory address counter cleared to 0	
3?5	**22**		**CPU Latch Data (CR22)**	**16-24**
	7-0	R	Value in the CPU latch in the graphics controller	
3?5	**24,26**		**Attribute Controller Flag/Index**	**16-25**
	5-0	R	Value of the attribute controller index data at 3C0H	
	6	R	Reserved	
	7	R	State of inverted internal address flip-flop	

Table B-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
Graphics Controller Registers				
3CE			**Graphics Controller Index**	**16-26**
	3-0	R/W	Index to the graphics controller register to be accessed	
	7-4	R/W	Reserved	
3CF			**Graphics Controller Data**	**16-26**
	7-0	R/W	Data to or from the graphics controller register accessed	
3CF	**00**		**Set/Reset (GR0)**	**16-27**
	3-0	R/W	Color value for CPU memory writes	
	7-4	R/W	Reserved	
3CF	**01**		**Enable Set/Reset (GR1)**	**16-27**
	3-0	R/W	Enable planes for writing GR0 data	
	7-4	R/W	Reserved	
3CF	**02**		**Color Compare (GR2)**	**16-28**
	3-0	R/W	Reference color for color compare operations	
	7-4	R/W	Reserved	
3CF	**03**		**Raster Operation/Rotate Counter (GR3)**	**16-28**
	2-0	R/W	Number of right rotate positions for a CPU memory write	
	4-3	R/W	Select raster operation (logical function)	
	7-5	R/W	Reserved	
3CF	**04**		**Read Plane Select (GR4)**	**16-29**
	1-0	R/W	Select planes for reading	
	7-2	R/W	Reserved	
3CF	**05**		**Graphics Controller Mode (GR5)**	**16-30**
	1-0	R/W	Select write mode	
	2	R/W	Reserved	
	3	R/W	Enable read compare operation	
	4	R/W	Select odd/even addressing	
	5	R/W	Select odd/even shift mode	
	6	R/W	Select 256 color shift mode	
	7	R/W	Reserved	
3CF	**06**		**Memory Map Mode Control (GR6)**	**16-31**
	0	R/W	Select graphics mode memory addressing	
	1	R/W	Chain odd/even planes	
	3-2	R/W	Select memory mapping	
	7-4	R/W	Reserved	
3CF	**07**		**Color Don't Care (GR7)**	**16-32**
	3-0	R/W	Select color plane used for color comparison	
	7-4	R/W	Reserved	

Table B-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3CF	**08**		**Bit Mask (GR8)**	**16-32**
	7-0	R/W	Each bit is a mask for the corresponding memory plane bit	
Attribute Registers				
3C0			**Attribute Controller Index**	**16-33**
	4-0	R/W	Index to the attribute controller register to be accessed	
	5	R/W	Enable video display	
	7-6	R/W	Reserved	
3C1/0			**Attribute Controller Data**	**16-34**
	7-0	R/W	Data to or from the attribute controller register accessed	
3C1/0	**00–0F**		**Palette Register (AR0–ARF)**	**16-34**
	5-0	R/W	Color value	
	7-6	R/W	Reserved	
3C1/0	**10**		**Attribute Mode Control (AR10)**	**16-35**
	0	R/W	Select graphics mode	
	1	R/W	Select monochrome display	
	2	R/W	Enable line graphics characters	
	3	R/W	Enable blinking	
	4	R/W	Reserved	
	5	R/W	Enable top panning	
	6	R/W	Select 256 color mode	
	7	R/W	Bits 5-4 of video output come from AR14_1-0	
3C1/0	**11**		**Border Color (AR11)**	**16-36**
	7-0	R/W	Border color value	
3C1/0	**12**		**Color Plane Enable (AR12)**	**16-36**
	3-0	R/W	Display plane enable	
	5-4	R/W	Select inputs to bits 5-4 of 3?AH	
	7-6	R/W	Reserved	
3C1/0	**13**		**Horizontal Pixel Panning (AR13)**	**16-37**
	3-0	R/W	Number of pixels to shift the display to the left	
	7-4	R/W	Reserved	
3C1/0	**14**		**Pixel Padding (AR14)**	**16-38**
	1-0	R/W	Bits 5-4 of the video output if AR10_7 = 1	
	3-2	R/W	Bits 7-6 of the video output	
	7-4	R/W	Reserved	

Table B-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
RAMDAC Registers				
3C6			**DAC Mask**	**16-39**
	7-0	R/W	Pixel read mask	
3C7			**DAC Read Index**	**16-39**
	7-0	W	Index to palette register to be read	
3C7			**DAC Status**	**16-40**
	1-0	R	Shows whether previous DAC cycle was a read or write	
	7-2	R	Reserved	
3C8	–		**DAC Write Index**	**16-40**
	7-0	R/W	Index to palette register to be written	
3C9			**DAC Data**	**16-41**
	7-0	R/W	Data from register pointed to by DAC Read or Write Index	

B.2 EXTENDED SEQUENCER REGISTERS

Table B-2. Extended Sequencer Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**08**		**Unlock Extended Sequencer (SR8)**	**17-1**
	7-0	R/W	Load xxxx0110b to unlock SR9-SR1C	
3C5	**09**		**Extended Sequencer 9 (SR9)**	**17-2**
	0	R/W	Reserved	
	1	R/W	Engine clock off when engine not busy	
	2	R/W	Controller 1 virtual DCLK off when CR67_3-2 = 11b	
	3	R/W	Controller 1 virtual DCLK off in Standby	
	4	R/W	Controller 1 virtual DCLK off in Suspend	
	5	R/W	Controller 1 true DCLK off in Standby	
	6	R/W	Controller 1 true DCLK off in Suspend	
	7	R/W	MMIO-only	
3C5	**0A**		**Extended Sequencer A (SRA)**	**17-3**
	0	R/W	AD[31:0] output drive strength	
	1	R/W	Reserved	
	2	R/W	Enable 16 BPP fix	
	3	R/W	Enable 24 BPP Alpha Blending fix	
	4	R/W	Delay when switching between 2D/3D commands	
	5	R/W	Delay rectangle or line after a 3D command	
	6	R/W	Extend S3d engine busy signal	
	7	R/W	Reserved	
3C5	**0D**		**DCLK2 Control (SRB)**	**17-4**
	0	R/W	DCLK2 PLL powered down	
	1	R/W	Load new DCLK2 frequency	
	2	R/W	Select DCLK to output	
	3	R/W	PLL test (test only)	
	4	R/W	Divide Controller 2 dot clock by 2	
	5	R/W	Select reference clock for DCLK2 PLL	
	6	R/W	Invert DCLK2 in clock doubled mode	
	7	R/W	Select external DCLK2 source on EDCLK2 pin	
3C5	**0D**		**Extended Sequencer D (SRD)**	**17-5**
	0	R/W	LPBEN pin is held at logic 1	
	2-1	R/W	Reserved	
	3	R/W	Force LBP disable	
	5-4	R/W	HSYNC control for Green PC requirements	
	7-6	R/W	VSYNC control for Green PC requirements	

Table B-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**12**		**Enhanced Modc DCLK2 Value Low (SRE)**	**17-6**
	5-0	R/W	DCLK2 N-divider value	
	7-6	R/W	DCLK2 R value	
3C5	**13**		**Enhanced Mode DCLK2 Value High (SRF)**	**17-6**
	7-0	R/W	DCLK2 M-divider value	
3C5	**10**		**MCLK Value Low (SR10)**	**17-7**
	4-0	R/W	MCLK N-divider value	
	6-5	R/W	MCLK R value	
	7	R/W	Reserved	
3C5	**11**		**MCLK Value High (SR11)**	**17-7**
	6-0	R/W	MCLK M-divider value	
	7	R/W	Reserved	
3C5	**12**		**Enhanced Mode DCLK2 Value Low (SR12)**	**17-8**
	4-0	R/W	DCLK1 N-divider value	
	5	R/W	Reserved	
	7-6	R/W	DCLK1 R value	
3C5	**13**		**Enhanced Mode DCLK1 Value High (SR13)**	**17-9**
	6-0	R/W	DCLK1 M-divider value	
	7	R/W	Reserved	
3C5	**14**		**Clock Synthesizer Control 1 (SR14)**	**17-9**
	0	R/W	DCLK PLL powered down (test only)	
	1	R/W	MCLK PLL powered down (test only)	
	2	R//w	Enable clock synthesizer test counter	
	3	R/W	Select MCLK or DCLK for test	
	4	R/W	Clear clock synthesizer test counters	
	5	R/W	LPBEN pin is tri-stated	
	6	R/W	MCLK is input on LPBEN pin (test only)	
	7	R/W	DCLK1 is input on XIN pin (test only)	
3C5	**15**		**Clock Synthesizer Control 2 (SR15)**	**17-11**
	0	R/W	Load new MCLK frequency	
	1	R/W	Load new DCLK1 frequency	
	2	R/W	MCLK output on STWR/GOP0 pin (test only)	
	3	R/W	DCLK1 output on LCLK pin (test only)	
	4	R/W	Divide DCLK1 by 2	
	5	R/W	Load MCLK and DCLK PLL values immediately	
	6	R/W	Invert DCLK1 in clock doubled mode	
	7	R/W	Enable 1 MCLK CPU memory writes	
3C5	**16**		**CLKSYN Test High (SR16)**	**17-12**
	7-0	R	High byte of clock synthesizer test results	

Table B-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**17**		**CLKSYN Test Low (SR17)**	**17-12**
	7-0	R	Low byte of clock synthesizer test results	
3C5	**18**		**RAMDAC/CLKSYN Control (SR18)**	**17-13**
	0	R/W	RAMDAC signature test counter enabled	
	1	R/W	Reset RAMDAC signature test counter	
	2	R/W	Place signature test blue data on internal data bus	
	3	R/W	Place signature test green data on internal data bus	
	4	R/W	Place signature test red data on internal data bus)	
	5	R/W	Power-down RAMDAC	
	6	R/W	Select 1 cycle CLUT write	
	7	R/W	RAMDAC clock doubled mode enabled	
3C5	**19**		**TV DAC Control (SR19)**	**17-14**
	2-0	R/W	Reserved	
	3	R/W	TV DAC test mode (test only)	
	4	R/W	Enable TV DAC SENSE circuit	
	5	R/W	TV DAC power down	
	7-6	R/W	Reserved	
3C5	**1A**		**Extended Sequencer 1A (SR1A)**	**17-15**
	0	R/W	Filter capacitor test (test only)	
	1	R/W	Filter capacitor test mode (test only)	
	3-2	R/W	Filter capacitor test select (test only)	
	4	R/W	Select function ofSTWR/GOP0 pin	
	5	R/W	Reserved	
	6	R/W	Power down internal oscillator	
	7	R/W	TV DAC output level control	
3C5	**1B**		**Extended Sequencer 1B (SR1B)**	**17-16**
	0	R/W	Reserved	
	1	R	TV DAC Y SENSE	
	2	R	TV DAC C SENSE	
	6-3	R/W	Reserved	
	7	R/W	Force Controller 1 DCLK source	
3C5	**1C**		**Extended Sequencer 1C (SR1C)**	**17-16**
	1-0	R/W	DCLK control for TV modes	
	2	R/W	TV encoder clock off when encoder disabled	
	3	R/W	TV encoder clock off in Standby	
	4	R/W	TV encoder clock off in Suspend	
	5	R/W	LCLK off when LPB disabled	
	6	R/W	LCLK off in Standby	
	7	R/W	LCLK off in Suspend	

Table B-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**1D**		**Extended Sequencer 1D (SR1D)**	**17-17**
	2-0	R/W	Reserved	
	3	R/W	SP DCLK off when SP disabled	
	4	R/W	SP DCLK off in Standby	
	5	R/W	SP DCLK off in Suspend	
	7-6	R/W	Reserved	
3C5	**1E**		**Extended Sequencer 1E (SR1E)**	**17-18**
	0	R/W	Controller 1 DCLK off when Controller 1 disabled	
	1	R/W	Reserved	
	2	R/W	Controller 2 DCLK off when Controller 2 disabled	
	3	R/W	Controller 2 DCLK off in Standby	
	4	R/W	Controller 2 DCLK off in Suspend	
	6-5	R/W	Reserved	
	7	R/W	Bus interface SCLK off in Suspend	
3C5	**1F**		**Extended Sequencer 1F (SR1F)**	**17-19**
	0	R/W	S3d MCLK off in Suspend	
	1	R/W	Non-S3d MCLK off in Suspend	
	3-2	R/W	Reserved	
	4	R/W	Memory interface 5V tolerant	
	5	R/W	CPU interface 5V tolerant	
	6	R/W	LPB/CRT interface 5V tolerant	
	7	R/W	Flat panel interface pull-up control	
3C5	**20**		**Extended Sequencer 20 (SR20)**	**17-20**
	0	R/W	DCLK2 off in Suspend	
	1	R/W	CRT DAC off in Standby	
	2	R/W	CRT DAC off in Suspend	
	3	R/W	DCLK1 PLL off in Suspend	
	4	R/W	MCLK PLL off in Suspend	
	5	R/W	TV DAC off in Standby	
	6	R/W	TV DAC off in Suspend	
	7	R/W	Pads in suspend configuration in Suspend	

Table B-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**21**		**Extended Sequencer 21 (SR21)**	**17-21**
	0	R/W	Disable CLUT1	
	1	R/W	Disable monitor sense circuit	
	2	R/W	Controller 1 CLUT powered down in Standby	
	3	R/W	Controller 1 CLUT powered down in Suspend	
	4	R/W	Disable CLUT2	
	5	R/W	Contrller 2 CLUT powered down when Controller 2 diasabled	
	6	R/W	Controller 2 CLUT powered down in Standby	
	7	R/W	Controller 2 CLUT powered down in Suspend	
3C5	**22**		**VGA Clock 1 Value Low (SR22)**	**17-22**
	4-0	R/W	VGA Clock 1 N-divider value	
	5	R/W	Reserved	
	7-6	R/W	VGA Clock 2 R value	
3C5	**23**		**VGA Clock 1 Value High (SR23)**	**17-23**
	6-0	R/W	VGA Clock 1 M-divider value	
	7	R/W	Reserved	
3C5	**24**		**VGA Clock 2 Value Low (SR24)**	**17-23**
	4-0	R/W	VGA Clock 2 N-divider value	
	5	R/W	Reserved	
	7-6	R/W	VGA Clock 2 R value	
3C5	**25**		**VGA Clock 2 Value High (SR25)**	**17-24**
	6-0	R/W	VGA Clock 2 M-divider value	
	7	R/W	Reserved	
3C5	**26**		**Paired Register Read/Write Select (SR26)**	**17-24**
	0	R/W	Certain CRTC register reads are disabled for Controller 1	
	1	R/W	Reads of all paired Controller 1 registers are disabled	
	2	R/W	Enable writes to Controller 2 registers	
	3	R/W	Disable writes to Controller 1 registers	
	5-4	R/W	Reserved	
	6	R/W	CLUT1 power down control	
	7	R/W	Select vertical interrupt controller source	
3C5	**27**		**DAC Current Control (SR27)**	**17-26**
	2-0	R/W	CRT DAC gain adjust	
	3	R/W	Enable BLANK pedestal	
	6-4	R/W	TV DAC gain adjust	
	7	R/W	Reserved	

Table B-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**28**		**PLL IREF Control (SR28)**	**17-26**
	1-0	R/W	MCLK IREF current adjust	
	3-2	R/W	DCLK1 IREF current adjust	
	5-4	R/W	DCLK2 IREF current adjust	
	7-6	R/W	Reserved	
3C5	**29**		**DCLK PLL Value Overflow (SR29)**	**17-27**
	0	R/W	DCLK1 PLL R value bit 2	
	1	R/W	Reserved	
	2	R/W	DCLK2 PLL R value bit 2	
	3	R/W	DCLK2 PLL M value bit 8	
	4	R/W	DCLK2 PLL N value bit 6	
	7-5	R/W	Reserved	

B.3 EXTENDED CRTC REGISTERS

All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 1 register (CR38) must be loaded with a binary unlock key pattern (see the register description). CTR registers are unlocked by setting CR39 = A5H. The registers will remain unlocked until the key pattern is reset. ? = B for monochrome, D for color.

Table B-3. Extended CRTC Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**22**	R/W	**CRT Test 1(CTR22)**	**18-1**
	6-0	R/W	Reserved	
	7	R/W	Provide pixel data to DAC (Test) - Paired	
3?5	**23**	R/W	**Synchronization 1(CTR23)**	**18-2**
	7-0	R/W	Reserved (always leave at 00H)	
3?5	**26**	R/W	**Synchronization 1(CTR26)**	**18-2**
	7-0	R/W	Write anything to this register before enabling vertical interpolation.	
3?5	**2D**		**Device ID High (CR2D)**	**18-2**
	7-0	R	High byte of device ID (8CH)	
3?5	**2E**		**Device ID Low (CR2E)**	**18-3**
	7-0	R	Low byte of device ID (01H)	
3?5	**2F**		**Revision (CR2F)**	**18-3**
	7-0	R	xx (varies with revision)	
3?5	**30**		**Chip ID/Rev (CR30)**	**18-3**
	7-0	R	Chip Identification - E1H	
3?5	**31**		**Memory Configuration (CR31)**	**18-4**
	0	R/W	Enable CPU base address offset	
	1	R/W	Enable two-page screen image	
	2	R/W	Enable VGA 16-Bit Memory Bus Width	
	3	R/W	Use Enhanced mode memory mapping	
	5-4	R/W	Reserved	
	6	R/W	Enable high speed text display font fetch mode	
	7	R/W	Reserved	
3?5	**32**		**Backward Compatibility 1 (CR32)**	**18-5**
	1-0	R/W	Reserved	
	2	R/W	Force internal dot clock to be not divided by 2	
	3	R/W	Reserved	
	4	R/W	Enable interrupt generation	
	5	R/W	Reserved	
	6	R/W	Standard VGA memory wrap at 256K boundary	
	7	R/W	Reserved	

Table B-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**33**		**Backward Compatibility 2 (CR33)**	**18-6**
	0	R	Controller in active display area status - Paired	
	1	R/W	Disable write protection provided by CR11_7 on CR7_1,6	
	2	R	Vertical sync active status - Paired	
	3	R/W	VCLK is inverted DCLK - Paired	
	4	R/W	Disable writes to RAMDAC registers (3C6H-3C9H)	
	5	R/W	BLANK signal active during non-active video period - Paired	
	6	R/W	Disable writes to AR0-ARF registers - Paired	
	7	R	Current flicker filter odd/even field status - Paired	
3?5	**34**		**Backward Compatibility 3 (CR34)**	**18-7**
	0	R/W	PCI DAC snoop method select	
	1	R/W	Disable PCI master abort handling during DAC snoop	
	2	R/W	Disable PCI retry handling during DAC snoop	
	4-3	R/W	Reserved	
	5	R/W	Force to 8 dots/character text mode	
	6	R/W	Reserved	
	7	R/W	Lock 3C2H_3-2 (DCLK select)	
3?5	**35**		**CRT Register Lock (CR35) - Paired**	**18-8**
	3-0	R/W	Reserved	
	4	R/W	Lock Vertical Timing registers - Paired	
	5	R/W	Lock Horizontal Timing registers - Paired	
	6	R/W	Lock CR1 and 3C2H_6	
	7	R/W	Lock CR12 and 3C2H_7	
3?5	**36**		**Configuration 1 (CR36)**	**18-9**
	0	R/W	Reserved	
	1	R/W	Use external MCLK on LPBEN pin	
	3-2	R/W	Select memory type (SDRAM/SGRAM or 1-cycle EDO)	
	5-4	R/W	Reserved	
	7-6	R/W	Define display memory size	
3?5	**37**		**Configuration 2 (CR37)**	**18-9**
	0	R/W	Disable I/O accesses	
	1	R/W	NAND tree test enable	
	2	R/W	Subsytem ID data source	
	3	R/W	Use internal/external MCLK, DCLK	
	4	R/W	Reserved	
	7-5	R/W	Define panel type	

Table B-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**38**		**Register Lock 1 (CR38)**	**18-11**
	7-0	R/W	Unlock S3 VGA registers (CR2D-CR3F)	
3?5	**39**		**Register Lock 2 (CR39)**	**18-11**
	7-0	R/W	Unlock System Control and System Extension registers	
3?5	**3A**		**Miscellaneous 1 (CR3A)**	**18-11**
	2-0	R/W	Reserved	
	3	R/W	Enable simultaneous VGA text and Enhanced modes - Paired	
	4	R/W	Enable 8-, 16- or 24/32-bit color Enhanced modes - Paired	
	5	R/W	Enable high speed text font writing	
	6	R/W	Reserved	
	7	R/W	Disable PCI bus read burst cycles	
3?5	**3B**		**Start Display FIFO Fetch (CR3B) - Paired**	**18-12**
	7-0	R/W	Specify start of display FIFO fetches for screen refreshing	
3?5	**3C**		**Interlace Retrace Start (CR3C) - Paired**	**18-13**
	7-0	R/W	Specify interlaced mode retrace start position	
3?5	**3D**		**NTSC/PAL Control (CR3D)**	**18-13**
	0	R/W	Enable TV mode	
	2-1	R/W	Select TV output	
	3	R/W	Reserved	
	4	R/W	Select black and white video	
	5	R/W	Select NTSC or PAL	
	6	R/W	Composite sync on VSYNC pin	
	7	R/W	Select U.S. vs Japanese NTSC	
3?5	**3E**		**Vertical Counter (CR3E)**	**18-14**
	7-0	R/W	Specify interlaced mode retrace start position	

Table B-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**40**		**System Configuration (CR40)**	**18-14**
	0	R/W	Reserved = 0	
	7-1	R/W	Reserved	
3?5	**41**		**BIOS Flag (CR41)**	**18-15**
	7-0	R/W	Used by the video BIOS	
3?5	**42**		**Mode Control (CR42)**	**18-15**
	4-0	R/W	Reserved	
	5	R/W	Select Interlaced mode - Paired	
	7-6	R/W	Reserved	
3?5	**43**		**Extended Mode (CR43) - Paired**	**18-15**
	2-0	R/W	Reserved	
	3	R/W	Select character blink rate	
	4	R/W	Reserved	
	6-5	R/W	Select cursor blink rate	
	7	R/W	Enable horizontal counter double mode	
3?5	**45**		**Hardware Graphics Cursor Mode (CR45)**	**18-16**
	0	R/W	Enable hardware graphics cursor	
	1	R/W	Hardware cursor position change control	
	3-2	R/W	Reserved	
	4	R/W	Set up space at right of bit map for hardware cursor	
	7-5	R/W	Reserved	
3?5	**46–47**		**Hardware Graphics Cursor Origin-X (CR46-CR47)**	**18-17**
	10-0	R/W	X-coordinate of the hardware cursor left side	
	15-11	R/W	Reserved	
3?5	**48–49**		**Hardware Graphics Cursor Origin-Y (CR48-CR49)**	**18-17**
	10-0	R/W	Y-coordinate of the hardware cursor upper line	
	15-11	R/W	Reserved	
3?5	**4A**		**Hardware Graphics Cursor Foreground Stack (CR4A)**	**18-17**
	7-0	R/W	Hardware cursor foreground color (3 registers)	
3?5	**4B**		**Hardware Graphics Cursor Background Stack (CR4B)**	**18-18**
	7-0	R/W	Hardware cursor background color (3 registers)	
3?5	**4C–4D**		**Hardware Graphics Cursor Start Address (CR4C-CR4D)**	**18-18**
	12-0	R/W	Hardware cursor start address	
	15-13	R/W	Reserved	
3?5	**4E**		**Hardware Graphics Cursor Pattern Display Start X-Pixel Position (CR4E)**	**18-18**
	5-0	R/W	Hardware cursor display start x-coordinate	
	7-6	R/W	Reserved	

Table B-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**4F**		**Hardware Graphics Cursor Pattern Display Start Y-Pixel Position (CR4F)**	**18-19**
	5-0	R/W	Hardware cursor display start y-coordinate	
	7-6	R/W	Reserved	
3?5	**50**		**Software (CR50)**	**18-19**
	3-0	R/W	Reserved for S3 software	
3?5	**51**		**Extended System Cont 2 (CR51) - Paired**	**18-19**
	3-0	R/W	Reserved	
	5-4	R/W	Logical screen width bits 9-8	
	6	R/W	Reserved	
	7	R/W	Streams Processor shadow register load control	
3?5	**52**		**Extended BIOS Flag 1 (CR52)**	**18-20**
	7-0	R/W	Used by the video BIOS	
3?5	**53**		**Extended Memory Cont 1 (CR53)**	**18-20**
	0	R/W	Reserved	
	2-1	R/W	Big endian byte swap select for linear addressing	
	4-3	R/W	Memory-mapped I/O type select	
	5	R/W	MMIO window select (A8000H or B8000H)	
	6	R/W	Enable nibble swap	
	7	R/W	Reserved	
3?5	**54**		**Extended Memory Cont 2 (CR54)**	**18-21**
	1-0	R/W	Big endian byte swap select (not linear addressing or image transfers)	
	7-2	R/W	Reserved	
3?5	**55**		**Extended DAC Control (CR55)**	**18-22**
	4-0	R/W	Reserved	
	5	R/W	Enable hardware cursor/icon display	
	7-6	R/W	Reserved	
3?5	**56**		**External Sync Cont 1 (CR56)**	**18-22**
	0	R/W	Reserved	
	1	R/W	HSYNC output buffer tri-stated	
	2	R/W	VSYNC output buffer tri-stated	
	7-3	R/W	Reserved	

Table B-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**58**		**Linear Address Window Control (CR58)**	**18-23**
	1-0	R/W	Linear addressing window size	
	3-2	R/W	Reserved	
	4	R/W	Enable linear addressing for Enhanced modes	
	7-5	R/W	Reserved	
3?5	**59-5A**		**Linear Address Window Position (CR59-5A)**	**18-24**
	15-0	R/W	Linear addressing window position bits 31-16	
3?5	**5C**		**General Out Port (CR5C)**	**18-25**
	7-0	R/W	General Output Port	
3?5	**5D**		**Extended Horizontal Overflow (CR5D) - Paired**	**18-25**
	0	R/W	Horizontal total bit 8 (CR0)	
	1	R/W	Horizontal display end bit 8 (CR1)	
	2	R/W	Start horizontal blank bit 8 (CR2)	
	3	R/W	Horizontal blank period is greater than 64 character clocks	
	4	R/W	Start horizontal sync position bit 8 (CR4)	
	5	R/W	Horizontal sync period is greater than 32 character clocks	
	6	R/W	Start FIFO Fetch bit 8 (CR3B)	
	7	R/W	Reserved	
3?5	**5E**		**Extended Vertical Overflow (CR5E) - Paired**	**18-26**
	0	R/W	Vertical total bit 10 (CR6)	
	1	R/W	Vertical display end bit 10 (CR12)	
	2	R/W	Start vertical blank bit 10 (CR15)	
	3	R/W	Reserved	
	4	R/W	Vertical retrace start bit 10 (CR10)	
	5	R/W	Reserved	
	6	R/W	Line compare position bit 10 (CR18)	
	7	R/W	Reserved	
3?5	**60**		**Extended Memory Control 3 (CR60)**	**18-26**
	3-0	R/W	SDCLK timing control	
	7-4	R/W	Reserved	
3?5	**61**		**Extended Memory Control 4 (CR61)**	**18-27**
	4-0	R/W	Reserved	
	6-5	R/W	Big endian byte swap select for image writes	
	7	R/W	Reserved	
3?5	**63**		**Start FIFO Fetch (CR63)**	**18-27**
	0	R/W	HSYNC timing type	
	2-1	R/W	Reserved	
	4-3	R/W	Start display FIFO fetch control	
	7-5	R/W	Reserved	

Table B-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**65**		**Extended Miscellaneous Control (CR65)- Paired**	**18-28**
	2-0	R/W	Reserved	
	4-3	R/W	Delay BLANK by DCLK - Paired	
	7-5	R/W	Reserved	
3?5	**66**		**Extended Miscellaneous Control 1 (CR66)**	**18-28**
	0	R/W	Enable enhanced functions - Paired	
	1	R/W	Software reset of the S3d Engine	
	2	R/W	Reserved	
	3	R/W	PCI disconnect on write with FIFO full or read with FIFO empty	
	4	R/W	Reserved	
	5	R/W	Streams Processor register load control	
	6	R/W	Enable linear addressing in non-Enhanced modes	
	7	R/W	Enable PCI bus disconnect	
3?5	**67**		**Extended Miscellaneous Control 2 (CR67)**	**18-29**
	1-0	R/W	Reserved	
	2	R/W	Streams Processor mode select	
	3	R/W	Reserved	
	7-4	R/W	Select RAMDAC color mode - Paired	
3?5	**68**		**Configuration 3 (CR68)**	**18-30**
	1-0	R/W	CAS stretch (EDO), auto refresh to command (SD/GRAM	
	2	R/W	Select edge to stretch for CAS, OE and WE	
	3	R/W	RAS low (EDO), SDRAS low (SD/GRAM)	
	5-4	R/W	RAS precharge (EDO), SDRAS precharge (SD/GRAM)	
	7-6	R/W	DRAM type select	
3?5	**69**		**Extended System Control 3 (CR69) - Paired**	**18-32**
	3-0	R/W	Display start address bits 19-16	
	7-4	R/W	Reserved	
3?5	**6A**		**Extended System Control 4 (CR6A)**	**18-32**
	5-0	R/W	CPU base address bits 19-14	
	7-6	R/W	Reserved	
3?5	**6B**		**Extended BIOS Flag 3 (CR6B)**	**18-32**
	7-0	R/W	Used by the video BIOS	
3?5	**6C**		**Extended BIOS Flag 4 (CR6C)**	**18-33**
	7-0	R/W	Used by the video BIOS	
3?5	**6D**		**Extended BIOS Flag 5 (CR6D)**	**18-33**
	7-0	R/W	Used by the video BIOS	
3?5	**6E**		**RAMDAC Signature Test Data**	**18-33**
	7-0	R/W	RAMDAC signature test data	

Table B-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**6F**		**Configuration 4 (CR6F)**	**18-34**
	0	R/W	Select function of FPPOL/ROMEN pin	
	1	R/W	Select I/O address for Serial Port register	
	2	R/W	Disable effect of bit 1 of this register	
	4-3	R/W	WE delay (EDO), miscellaneous SD/GRAM timing	
	6-5	R/W	OE delay (EDO, CAS latency (SD/GRAM)	
	7	R/W	Select SDCLK vs SDCLKI to latch read data	
3?5	**71**		**Extended Miscellaneous Control 2 (CR71) - Paired**	**18-35**
	0	R/W	Reserved	
	1	R/W	Screen off bit select	
	4-2	R/W	Reserved	
	5	R/W	Screen off	
	7-6	R/W	Reserved	
3?5	**72**		**Extended Memory Control 5 (CR72)**	**18-36**
	4-0	R/W	Reserved	
	5	R/W	SD/GRAM mode set	
	7-6	R/W	Reserved	
3?5	**74**		**Extended Memory Control 7 (CR74)**	**18-36**
	0	R/W	Disable distributed refresh	
	3-1	R/W	Memory refresh type during power down	
	4	R/W	Burst refresh before self refresh	
	5	R/W	Burst refresh after self refresh	
	7-6	R/W	Reserved	
3?5	**75**		**Extended Memory Control 8 (CR75)**	**18-37**
	7-0	R/W	Refresh count	
3?5	**76**		**Memory Cycle Control 1 (CR76)**	**18-38**
	0	R/W	Use 1-cycle linear addressing writes to video memory	
	7-1	R/W	Reserved	
3?5	**77**		**Memory Cycle Control 2 (CR77)**	**18-38**
	0	R/W	Reserved	
	1	R/W	SDCLK buffer strength	
	2	R/W	PD[63:0] buffer strength	
	3	R/W	MA[10:0] buffer strength	
	7-4	R/W	Reserved	
3?5	**78**		**Memory Timing Control (CR78)**	**18-39**
	0	R/W	Delay RAS rising edge by 0.5 MCLK	
	7-1	R/W	Reserved	

Table B-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**7B**		**Primary Stream 1 Timeout (CR7B)**	**18-39**
	7-0	R/W	Primary stream 1 timeout	
3?5	**7C**		**Primary Stream 2 Timeout (CR7C)**	**18-39**
	7-0	R/W	Primary stream 2 timeout	
3?5	**7D**		**Secondary Stream Timeout (CR7D)**	**18-40**
	7-0	R/W	Secondary stream timeout	
3?5	**7F**		**STN Read Timeout (CR7F)**	**18-40**
	7-0	R/W	STN read timeout	
3?5	**80**		**STN Write Timeout (CR80)**	**18-40**
	7-0	R/W	STN write timeout	
3?5	**81**		**LPB Write Timeout (CR81)**	**18-41**
	7-0	R/W	LPB write timeout	
3?5	**82**		**Read DMA Timeout (CR82)**	**18-41**
	7-0	R/W	Read DMA timeout	
3?5	**83**		**Host Interface Timeout (CR83)**	**18-41**
	7-0	R/W	Host interface timeout	
3?5	**84**		**S3d Engine Timeout (CR84)**	**18-42**
	7-0	R/W	S3d Engine timeout	
3?5	**85**		**Primary Stream 1 FIFO Threshold (CR85)**	**18-42**
	4-0	R/W	Primary stream 1 FIFO threshold	
	7-5	R/W	Reserved	
3?5	**86**		**Primary Stream 2 FIFO Threshold (CR86)**	**18-43**
	4-0	R/W	Primary stream 2 FIFO threshold	
	7-5	R/W	Reserved	
3?5	**87**		**Secondary FIFO Threshold (CR87)**	**18-43**
	4-0	R/W	Secondary stream FIFO threshold	
	7-5	R/W	Reserved	
3?5	**89**		**STN Read FIFO Threshold (CR89)**	**18-44**
	4-0	R/W	STN read FIFO threshold	
	7-5	R/W	Reserved	
3?5	**8A**		**STN Write FIFO Threshold (CR8A)**	**18-44**
	3-0	R/W	STN write FIFO threshold	
	7-6	R/W	Reserved	
3?5	**8B**		**LPB FIFO Threshold (CR8B)**	**18-45**
	4-0	R/W	LPB FIFO threshold	
	7-5	R/W	Reserved	

Table B-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**90**		**Primary Stream FIFO Fetch Control 1 (CR90) - Paired**	**18-45**
	2-0	R/W	Primary stream L1 parameter (10-8)	
	6-3	R/W	Reserved	
	7	R/W	Enable primary stream L1 parameter	
3?5	**91**		**Primary Stream FIFO Fetch Control 2 (CR91) - Paired**	**18-46**
	7-0	R/W	Primary stream L1 parameter (7-0)	
3?5	**92**		**Secondary Stream FIFO Fetch Control 1 (CR92)**	**18-46**
	2-0	R/W	Secondary stream L2 parameter (10-8)	
	6-3	R/W	Reserved	
	7	R/W	Enable secondary stream L2 parameter	
3?5	**93**		**Secondary Stream FIFO Fetch Control 2 (CR93)**	**18-47**
	7-0	R/W	Secondary stream L2 parameter (7-0)	
3?5	**95**		**PCI Subsystem Vendor ID Shadow Low (CR95)**	**18-47**
	7-0	R/W	PCI subsystem vendor ID low byte	
3?5	**96**		**PCI Subsystem Vendor ID Shadow High (CR96)**	**18-47**
	7-0	R/W	PCI subsystem vendor ID high byte	
3?5	**97**		**PCI Subsystem ID Shadow Low (CR97)**	**18-48**
	7-0	R/W	PCI subsystem ID low byte	
3?5	**98**		**PCI Subsystem ID Shadow High (CR98**	**18-48**
	7-0	R/W	PCI subsystem ID high byte	

B.4 S3D REGISTERS

This section lists the registers which support the S3d Engine functions. All of these registers are enabled only if bit 0 of CR40 is set to 1.

Table B-4. Color Pattern Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
			Color Pattern Registers	**19-3**
A100	31-0	R/W	First pattern register	
A104	31-0	R/W	Second pattern register	
.				
.				
.				
A1BC	31-0	R/W	Last pattern register	

Table B-5. S3D 2D Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
AxD4			**Source Base Address**	**19-4**
	2-0	R/W	Reserved = 0	
	21-3	R/W	Source base address	
	31-22	R/W	Reserved	
AxD8			**Destination Base Address**	**19-4**
	2-0	R/W	Reserved = 0	
	21-3	R/W	Destination base address	
	31-22	R/W	Reserved	
AxDC			**Left/Right Clipping**	**19-5**
	10-0	R/W	Left clipping limit	
	15-11	R/W	Reserved	
	26-16	R/W	Right clipping limit	
	31-27	R/W	Reserved	
AxE0			**Top/Bottom Clipping**	**19-6**
	10-0	R/W	Bottom clipping limit	
	15-11	R/W	Reserved	
	26-16	R/W	Top clipping limit	
	31-27	R/W	Reserved	

Table B-5. S3D 2D Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
AxE4			**Destination/Source Stride**	**19-6**
	11-0	R/W	Source stride	
	15-12	R/W	Reserved	
	27-16	R/W	Destination stride	
	31-28	R/W	Reserved	
AxE8			**Mono Pattern 0**	**19-7**
	31-0	R/W	Mono pattern 0	
AxEC			**Mono Pattern 1**	**19-7**
	31-0	R/W	Mono pattern 1	
AxF0			**Mono Pattern Background Color**	**19-8**
	7-0	R/W	Data 1	
	15-8	R/W	Data 2	
	23-16	R/W	Data 3	
	31-24	R/W	Reserved	
AxF4			**Mono Pattern Foreground Color**	**19-9**
	7-0	R/W	Data 1	
	15-8	R/W	Data 2	
	23-16	R/W	Data 3	
	31-24	R/W	Reserved	
A4F8			**Source Background Color**	**19-10**
	7-0	R/W	Data 1	
	15-8	R/W	Data 2	
	23-16	R/W	Data 3	
	31-24	R/W	Reserved	
A4FC			**Source Foreground Color**	**19-11**
	7-0	R/W	Data 1	
	15-8	R/W	Data 2	
	23-16	R/W	Data 3	
	31-24	R/W	Reserved	
Ax00			**Command Set**	**19-12**
	0	R/W	Enable autoexecute	
	1	R/W	Enable hardware clipping	
	4-2	R/W	Destination color format	
	5	R/W	Update screen with new pixel	
	6	R/W	Mono source	
	7	R/W	Image source data from CPU	
	8	R/W	Mono pattern	
	9	R/W	Transparent transfers	
	11-10	R/W	Image transfer alignment	

Table B-5. S3D 2D Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
Ax00			**Command Set (continued)**	**19-12**
	13-12	R/W	First doubleword offset for image transfers	
	16-14	R/W	Reserved	
	24-17	R/W	Select one of 256 ROPs	
	25	R/W	X positive BitBLT	
	26	R/W	Y positive BitBLT	
	30-27	R/W	2D command	
	31	R/W	Select 2D or 3D command	
A504			**Rectangle Width/Height**	**19-15**
	10-0	R/W	Rectangle height	
	15-11	R/W	Reserved	
	26-16	R/W	Rectangle width	
	31-27	R/W	Reserved	
A508			**Rectangle Source XY**	**19-15**
	10-0	R/W	Rectangle source Y	
	15-11	R/W	Reserved	
	26-16	R/W	Rectangle source X	
	31-27	R/W	Reserved	
A50C			**Rectangle Destination XY**	**19-16**
	10-0	R/W	Rectangle destination Y	
	15-11	R/W	Reserved	
	26-16	R/W	Rectangle destination X	
	31-27	R/W	Reserved	
A96C			**Line Draw Endpoints**	**19-17**
	15-0	R/W	End 1	
	31-16	R/W	End 2	
A970			**Line Draw X Delta**	**19-18**
	31-0	R/W	X delta	
A974			**Line Draw X Start**	**19-18**
	31-0	R/W	X start	
A978			**Line Draw Y Start**	**19-19**
	10-0	R/W	Y start	
	31-11	R/W	Reserved	

Table B-5. S3D 2D Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
A97C			**Line Draw Y Count**	**19-19**
	10-0	R/W	Scan line count	
	30-11	R/W	Reserved	
	31	R/W	Drawing direction from left to right	
AD68			**Polygon Right X Delta**	**19-20**
	31-0	R/W	Right edge X delta	
AD6C			**Polygon Right X Start**	**19-20**
	31-0	R/W	Right edge X start	
AD70			**Polygon Left X Delta**	**19-21**
	31-0	R/W	Left edge X delta	
AD74			**polygon left X Start**	**19-21**
	31-0	R/W	Left edge X start	
AD78			**Polygon Y Start**	**19-22**
	10-0	R/W	Top side of the clipping rectangle	
	31-11	R/W	Reserved	
AD7C			**Polygon Y Count**	**19-22**
	10-0	R/W	Scan line count	
	27-11	R/W	Reserved	
	28	R/W	Update right edge	
	29	R/W	Update left edge	
	31-30	R/W	Reserved	

Table B-6. S3D 3D Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
BxD4			**Z-Buffer Base Address**	**19-24**
	2-0	R/W	Reserved = 0	
	21-3	R/W	Z-buffer base address	
	31-22	R/W	Reserved	
BxD8			**Destination Base Address**	**19-24**
	2-0	R/W	Reserved = 0	
	21-3	R/W	Destination base address	
	31-22	R/W	Reserved	
BxDC			**Left/Right Clipping**	**19-25**
	10-0	R/W	Left clipping limit	
	15-11	R/W	Reserved	
	26-16	R/W	Right clipping limit	
	31-27	R/W	Reserved	
BxE0			**Top/Bottom Clipping**	**19-25**
	10-0	R/W	Bottom clipping limit	
	15-11	R/W	Reserved	
	26-16	R/W	Top clipping limit	
	31-27	R/W	Reserved	
BxE4			**Destination/Source Stride**	**19-26**
	12-0	R/W	Source stride	
	15-13	R/W	Reserved	
	28-16	R/W	Destination stride	
	31-29	R/W	Reserved	
BxE8			**Z-Stride**	**19-26**
	12-0	R/W	Z stride	
	31-13	R/W	Reserved	
BxEC			**Texture Base Address**	**19-27**
	2-0	R/W	Reserved = 0	
	21-3	R/W	Texture base address	
	31-22	R/W	Reserved	
B4F0			**Texture Border Color**	**19-27**
	7-0	R/W	Blue color index	
	15-8	R/W	Green color index	
	23-16	R/W	Red color index	
	31-24	R/W	Reserved	

Table B-6. S3D 3D Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
BxF4			**Fog Color**	**19-28**
	7-0	R/W	Blue color index	
	15-8	R/W	Green color index	
	23-16	R/W	Red color index	
	31-24	R/W	Reserved	
B4F8			**Color0**	**19-29**
	7-0	R/W	Blue color index	
	15-8	R/W	Green color index	
	23-16	R/W	Red color index	
	31-24	R/W	Reserved	
B4FC			**Color1**	**19-29**
	7-0	R/W	Data 1	
	15-8	R/W	Data 2	
	23-16	R/W	Data 3	
	31-24	R/W	Reserved	
Bx00			**Command Set**	**19-30**
	0	R/W	Enable autoexecute	
	1	R/W	Enable hardware clipping	
	4-2	R/W	Destination color format	
	7-5	R/W	Texel color format	
	11-8	R/W	MIPMAP level size	
	14-12	R/W	Texture filtering mode	
	16-15	R/W	Texture blending mode	
	17	R/W	Enable fogging	
	19-18	R/W	Alpha blending control	
	22-20	R/W	Z-buffer compare mode	
	23	R/W	Update z-buffer	
	25-24	R/W	Z-buffering mode	
	26	R/W	Enable texture wrapping	
	30-27	R/W	3D command	
	31	R/W	Select 2D or 3D command	

Table B-6. S3D 3D Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
B144			**3D Line Draw GB Delta**	**19-33**
	15-0	R/W	Blue delta	
	31-16	R/W	Green delta	
B148			**3D Line Draw AR Delta**	**19-33**
	15-0	R/W	Red delta	
	31-16	R/W	Alpha delta	
B14C			**3D Line Draw GB Start**	**19-34**
	15-0	R/W	Blue start	
	31-16	R/W	Green start	
B150			**3D Line Draw AR Start**	**19-34**
	15-0	R/W	Red start	
	31-16	R/W	Alpha start	
B158			**3D Line Draw Z Delta**	**19-35**
	31-0	R/W	Z delta	
B15C			**3D Line Draw Z Start**	**19-35**
	31-0	R/W	Z start	
B16C			**3D Line Draw Endpoints**	**19-36**
	15-0	R/W	End 1	
	31-16	R/W	End 2	
B170			**3D Line Draw X Delta**	**19-36**
	31-0	R/W	X delta	
B174			**3D Line Draw X Start**	**19-37**
	31-0	R/W	X start	
B178			**3d Line Draw Y Start**	**19-37**
	10-0	R/W	Y start	
	31-11	R/W	Reserved	
B17C			**3d Line Draw Y Count**	**19-38**
	10-0	R/W	Scan line count	
	30-11	R/W	Reserved	
	31	R/W	Drawing direction is left to right	

Table B-6. S3D 3D Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
B504			**Triangle Base V**	**19-38**
	19-0	R/W	Base V	
	21-20	R/W	Reserved	
	31-22	R/W	L0 constant	
B508			**Triangle Base U**	**19-39**
	19-0	R/W	Base U	
	28-20	R/W	Reserved	
	31-29	R/W	S3d mode	
B50C			**Triangle WX Delta**	**19-39**
	31-0	R/W	WX delta	
B510			**Triangle WY Delta**	**19-40**
	31-0	R/W	WY delta	
B514			**Triangle W Start**	**19-40**
	31-0	R/W	W start	
B518			**Triangle DX Delta**	**19-41**
	31-0	R/W	DX delta	
B51C			**Triangle VX Delta**	**19-41**
	31-0	R/W	VX delta	
B520			**Triangle UX Delta**	**19-42**
	31-0	R/W	UX delta	
B524			**Triangle DY Delta**	**19-42**
	31-0	R/W	DY delta	
B528			**Triangle VY Delta**	**19-43**
	31-0	R/W	VY delta	
B52C			**Triangle UY Delta**	**19-43**
	31-0	R/W	UY delta	
B530			**Triangle D Start**	**19-44**
	31-0	R/W	D start	
B534			**Triangle V Start**	**19-44**
	31-0	R/W	V start	
B538			**Triangle U Start**	**19-45**
	31-0	R/W	U start	
B53C			**Triangle GBX Delta**	**19-45**
	15-0	R/W	Blue X delta	
	31-16	R/W	Green X delta	
B540			**Triangle ARX Delta**	**19-46**
	15-0	R/W	Red X delta	
	31-16	R/W	Alpha X delta	

Table B-6. S3D 3D Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
B544			**Triangle GBY Delta**	**19-46**
	15-0	R/W	Blue Y delta	
	31-16	R/W	Green Y delta	
B548			**Triangle ARY Delta**	**19-47**
	15-0	R/W	Red Y delta	
	31-16	R/W	Alpha Y delta	
B54C			**Triangle GB Start**	**19-47**
	15-0	R/W	Blue start	
	31-16	R/W	Green start	
B550			**Triangle AR Start**	**19-48**
	15-0	R/W	Red start	
	31-16	R/W	Alpha start	
B554			**Triangle ZX Delta**	**19-48**
	31-0	R/W	ZX delta	
B558			**Triangle ZY Delta**	**19-49**
	31-0	R/W	ZY delta	
B55C			**Triangle Z Start**	**19-49**
	31-0	R/W	Z start	
B560			**Triangle XY12 Delta**	**19-50**
	31-0	R/W	XY12 delta	
B564			**Triangle X12 End**	**19-50**
	31-0	R/W	X12 end	
B568			**Triangle XY01 Delta**	**19-51**
	31-0	R/W	XY01 delta	
B56C			**Triangle X01 End**	**19-51**
	31-0	R/W	X01 end	
B570			**Triangle XY02 Delta**	**19-52**
	31-0	R/W	XY02 delta	
B574			**Triangle X Start**	**19-52**
	31-0	R/W	X start	
B578			**Triangle Y Start**	**19-53**
	31-0	R/W	Y start	
B57C			**Triangle Y Count**	**19-53**
	10-0	R/W	Scan line count 12	
	15-11	R/W	Reserved	
	26-16	R/W	Scan line count 01	
	30-27	R/W	Reserved	
	31	R/W	Render the triangle from right to left	

B.5 STREAMS PROCESSOR REGISTERS

Table B-7. Streams Processor Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
8184			**Color/Chroma Key Control**	**20-1**
	7-0	R/W	B/V/Cr key value (lower bound for chroma)	
	15-8	R/W	G/U/Cb key value (lower bound for chroma)	
	23-16	R/W	R/Y key value (lower bound for chroma)	
	26-24	R/W	RGB color comparison precision	
	27	R/W	Streams test mode 1	
	28	R/W	Streams test mode 2	
	30-29	R/W	Keying mode	
	31	R/W	Select stream for keying	
8190			**Secondary Stream Control**	**20-2**
	11-0	R/W	DDA horizontal accumulator initial value	
	22-12	R/W	Reserved	
	23	R/W	Disable secondary stream horizontal filtering	
	26-24	R/W	Secondary stream input data format	
	27	R/W	Reserved	
	30-28	R/W	Secondary stream filter characteristics	
	31	R/W	Reserved	
8194			**Chroma Key Upper Bound**	**20-3**
	7-0	R/W	V/Cr key value (upper bound)	
	15-8	R/W	U/Cb key value (upper bound)	
	23-16	R/W	Y key value (upper bound)	
	31-24	R/W	Reserved	
8198			**Secondary Stream Stretch/Filter Constants**	**20-4**
	10-0	R/W	K1 horizontal scale factor	
	15-11	R/W	Reserved	
	26-16	R/W	K2 horizontal scale factor	
	31-27	R/W	Reserved	
819C			**Color Adjustment**	**20-4**
	7-0	R/W	Brightness control	
	12-8	R/W	Contrast control	
	14-13	R/W	Reserved	
	15	R/W	Enable brightness and contrast control	
	20-16	R/W	Hue and saturation factor 1	
	23-20	R/W	Reserved	
	28-24	R/W	Hue and saturation factor 2	
	30-29	R/W	Reserved	
	31	R/W	Enable hue and saturation control	

Table B-7. Streams Processor Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
81A0			**Blend Control**	**20-6**
	1-0	R/W	Reserved	
	5-2	R/W	Secondary stream blend coefficient	
	9-6	R/W	Reserved	
	13-10	R/W	Primary stream blend coefficient	
	31-14	R/W	Reserved	
81CC			**Double Buffer/LPB Support**	**20-7**
	0	R/W	Reserved	
	2-1	R/W	Select secondary frame buffer address	
	3	R/W	Enable deintelacing	
	4	R/W	Select LPB frame buffer start address 1	
	5	R/W	LPB input buffer select loading at end of frame	
	6	R/W	Selected LPB input buffer toggles at end of frame	
	7	R/W	Synchronize secondary stream buffer address for deinterlacing	
	31-8	R/W	Reserved	
81D0			**Secondary Stream Frame Buffer Address 0**	**20-8**
	21-0	R/W	Secondary stream frame buffer starting address 0	
	31-22	R/W	Reserved	
81D4			**Secondary Stream Frame Buffer Address 1**	**20-9**
	21-0	R/W	Secondary stream frame buffer starting address 1	
	31-22	R/W	Reserved	
81D8			**Secondary Stream Stride**	**20-9**
	11-0	R/W	Secondary stream stride	
	31-12	R/W	Reserved	

Table B-7. Streams Processor Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
81DC			**Blend Control**	**20-10**
	2-0	R/W	Reserved	
	12-3	R/W	Pixel stop fetch position	
	18-13	R/W	Reserved	
	28-19	R/W	Pixel start fetch position	
	29	R/W	Reserved	
	30	R/W	Reserved = 0	
	31	R/W	Enable opaque overlay control	
81E0			**K1 Vertical Scale Factor**	**20-11**
	10-0	R/W	K1 vertical scale factor	
	31-11	R/W	Reserved	
81E4			**K2 Vertical Scale Factor**	**20-11**
	10-0	R/W	K2 vertical scale factor	
	31-11	R/W	Reserved	
81E8			**DDA Vertical Accumulator Initial Value**	**20-12**
	11-0	R/W	DDA vertical accumulator initial value 0	
	13-12	R/W	Reserved	
	14	R/W	Bandwidth savings mode	
	15	R/W	Enable secondary stream vertical interpolation	
	27-16	R/W	DDA vertical accumulator initial value 1	
	28	R/W	DDA vertical accumulator initial value select	
	31-29	R/W	Reserved	
81F8			**Secondary Stream Window Start Coordinates**	**20-13**
	10-0	R/W	Secondary stream Y start	
	15-11	R/W	Reserved	
	26-16	R/W	Secondary stream X start	
	31-27	R/W	Reserved	
81FC			**Secondary Stream Window Size**	**20-13**
	10-0	R/W	Secondary stream height	
	15-11	R/W	Reserved	
	26-16	R/W	Secondary stream width	
	31-27	R/W	Reserved	

B.6 DMA REGISTERS

Table B-8. DMA Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
8220			**DMA Read Base Address**	**21-2**
	2-0	R/W	Reserved = 0	
	22-3	R/W	DMA read base address	
	31-23	R/W	Reserved	
8224			**DMA Read Stride/Width**	**21-3**
	1-0	R/W	Address tiling control	
	2	R/W	Reserved = 0	
	11-3	R/W	DMA read stride	
	15-12	R/W	Reserved	
	18-16	R/W	Reserved = 0	
	27-19	R/W	DMA read width	
	31-28	R/W	Reserved	
8580				**21-4**
	0	R/W	Reserved	
	1	R/W	Video DMA write	
	31-2	R/W	DMA starting memory address	
8584			**Video DMA Transfer Length**	**21-5**
	1-0	R/W	Reserved	
	23-2	R/W	DMA transfer length	
	31-24	R/W	Reserved	
8588			**Video DMA Transfer Length**	**21-5**
	0	R/W	Enable video/graphics DMA	
	31-1	R/W	Reserved	
8590			**Command DMA Base Address**	**21-6**
	0	R/W	Reserved	
	1	R/W	Specify 4/64 KByte buffer size	
	11-2	R/W	Reserved	
	31-12	R/W	Command DMA buffer base address	
8594			**Command DMA Write Pointer**	**21-7**
	1-0	RW	Reserved	
	15-2	R/W	Write pointer	
	16	R/W	Write pointer updated	
	31-17	R/W	Reserved	
8598			**DMA Read Pointer**	**21-7**
	1-0	R/W	Reserved	
	15-2	R/W	Read pointer	
	31-16	R/W	Reserved	

Table B-8. DMA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
859C			**Command DMA Enable**	**21-8**
	0	RW	Enable Command DMA	
	31-1	R/W	Reserved	

B.7 MISCELLANEOUS CONTROL REGISTERS

Table B-9. Miscellaneous Control Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
8504			**Subsystem Status**	**22-1**
	0	R	Controller 1 vertical sync interrupt generated	
	1	R	S3d Engine interrupt generated	
	2	R	Command FIFO overflow interrupt generated	
	3	R	Command FIFO empty interrupt generated	
	4	R	Host DMA done interrupt generated	
	5	R	Command DMA done interrupt generated	
	6	R	S3d FIFO empty interrupt generated	
	7	R	LPB interrupt generated	
	12-8	R	S3d FIFO slots free (Bits 4-0)	
	13	R	S3d Engine idle	
	15-14	R	S3d FIFO slots free (Bits 6-5)	
	16	R	Controller 2 vertical sync interrupt status	
	31-17	R	Reserved	
8504			**Subsystem Control**	**22-3**
	0	W	Controller 1 vertical sync interrupt cleared	
	1	W	S3d Engine interrupt cleared	
	2	W	Command FIFO overflow interrupt cleared	
	3	W	Command FIFO empty interrupt cleared	
	4	W	Host DMA done interrupt cleared	
	5	W	Command DMA done interrupt cleared	
	6	W	S3d FIFO empty interrupt cleared	
	7	W	Host DMA done interrupt enabled	
	8	W	Controller 1 vertical sync interrupt enabled	
	9	W	S3d Engine interrupt enabled	
	10	W	Command FIFO overflow interrupt enabled	
	11	W	Command FIFO empty interrupt enabled	
	12	W	Command DMA done interrupt enabled	
	13	W	S3d FIFO empty interrupt enabled	
	15-14	W	S3d Engine software reset select	
	16	W	Reserved	
	17	W	Controller 2 vertical sync interrupt enabled	
	31-18	W	Reserved	

Table B-9. Miscellaneous Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
850C			**Advanced Function Control**	**22-5**
	0	R/W	Enable accelerated modes (enhanced and VESA non-planar)	
	3-1	R/W	Reserved	
	4	R/W	Enable linear addressing	
	5	R/W	Reserved	
	9-6	R	BIU FIFO Status	
	31-10	R/W	Reserved	

B.8 LOCAL PERIPHERAL BUS REGISTERS

Table B-10. Local Peripheral Bus Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
FF00			**LPB Mode**	**23-1**
	0	R/W	Enable LPB	
	3-1	R/W	LPB mode	
	4	R/W	Reset LPB	
	5	R/W	Write every other received frame to memory	
	6	R/W	No byte swap for incoming video	
	7	R/W	Select horizontal decimation mode	
	8	R/W	Reserved	
	9	R/W	LPB vertical sync is active high	
	10	R/W	LPB horizontal sync is active high	
	11	W	CPU VSYNC	
	12	W	CPU HSYNC	
	13	W	Load base address currently pointed to	
	15-14	R/W	Reserved	
	17-16	R/W	Maximum compressed data bust size	
	18	R/W	Reserved	
	19	R/W	Capture data when VS is high	
	20	R/W	Flush FIFO on early HREF	
	23-21	R/W	Reserved	
	24	R/W	LPB clock driven by LCLK	
	25	R/W	Don't add stride after first HSYNC	
	26	R/W	Invert the LCLK input	
	27	R/W	LPB base address select status	
	28	R/W	Odd/even frame status	
	29	R/W	Invert odd/even frame indicator	
	31-30	R/W	Base address select/enable ZV-Port	

Table B-10. Local Peripheral Bus Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
FF04			**LPB FIFO Status**	**23-5**
	3-0	R	LPB output FIFO status	
	10-4	R	Reserved	
	11	R	LPB output FIFO full	
	12	R	LPB output FIFO empty	
	13	R	LPB output FIFO almost empty	
	19-14	R	Reserved	
	20	R	LPB video FIFO full	
	21	R	LPB video FIFO empty	
	22	R	LPB video FIFO has 1 slot filled	
	31-23	R	Reserved	
FF08			**LPB Interrupt Flags**	**23-6**
	0	R/W	LPB Output FIFO empty	
	1	R/W	HSYNC (end of line) input	
	2	R/W	VSYNC (end of frame) input	
	3	R/W	Serial port start condition detected	
	6-4	R/W	Reserved	
	7	R/W	VSYNC trailing edge input	
	15-8	R/W	Reserved	
	16	R/W	Enable LPB output FIFO empty interrupt	
	17	R/W	Enable HSYNC (end of line) input interrupt	
	18	R/W	Enable VSYNC (end of frame) input interrupt	
	19	R/W	Enable serial port start condition detect interrupt	
	22-20	R/W	Reserved	
	23	R/W	Enable VSYNC trailing edge interrupt	
	24	R/W	Drive SPCLK low on receipt of a serial port start condition	
	31-25	R/W	Reserved	
FF0C			**LPB Frame Buffer Address 0**	**23-7**
	21-0	R/W	LPB frame buffer address 0	
	31-22	R/W	Reserved	
FF10			**LPB Frame Buffer Address 1**	**23-8**
	21-0	R/W	LPB frame buffer address 1	
	31-22	R/W	Reserved	
FF14			**LPB Direct Read/Write Address**	**23-8**
	20-0	R/W	Address of MPEG decoder address to read/write	
	31-21	R/W	Reserved	
FF18			**LPB Direct Read/Write Data**	**23-9**
	31-0	R/W	LPB direct read/write data	

Table B-10. Local Peripheral Bus Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
FF1C			**LPB General Purpose Input/Output Port**	**23-9**
	3-0	R/W	General purpose output data port	
	7-4	R	General purpose input data port	
	31-8	R/W	Reserved	
FF20			**Serial Port**	**23-10**
	0	R/W	0 = Serial clock write, 1 = tri-state	
	1	R/W	0 = Serial data write , 1 = tri-state	
	2	R	0 = Serial clock low, 1 = tri-state	
	3	R	0 = Serial data low, 1 = tri-state	
	4	R/W	Enable serial port function	
	5-7	R/W	Reserved	
	8	R	Bit 0 mirror (data on byte lane 2 at E2H)	
	9	R	Bit 1 mirror (data on byte lane 2 at E2H)	
	10	R	Bit 2 mirror (data on byte lane 2 at E2H)	
	11	R	Bit 3 mirror (data on byte lane 2 at E2H)	
	12	R	Bit 4 mirror (data on byte lane 2 at E2H)	
	31-13	R/W	Reserved	
FF24			**LPB Video Input Window Size**	**23-11**
	11-0	R/W	Video input line width	
	15-12	R/W	Reserved	
	24-16	R/W	Video input window height	
	31-25	R/W	Reserved	
FF28			**LPB Video Data Offsets**	**23-12**
	11-0	R/W	Horizontal video data offset	
	15-12	R/W	Reserved	
	24-16	R/W	Vertical video data offset	
	31-25	R/W	Reserved	
FF2C			**LPB Horizontal Decimation Control**	**23-12**
	31-0	R/W	Video data byte mask	
FF30			**LPB Vertical Decimation Control**	**23-13**
	7-0	R	Video data line mask	
FF34			**LPB Line Stride**	**23-13**
	11-0	R/W	Line stride	
	31-12	R/W	Reserved	
FF40			**LPB Output FIFO**	**23-14**
	31-0	R/W	Output FIFO data	

B.9 PCI CONFIGURATION SPACE REGISTERS

When a PCI configuration read or write command is issued, AD[7:0] contain the address of the register in the configuration space to be accessed.

Table B-11. PCI Configuration Space Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
00			**Vendor ID**	**24-1**
	15-0	R	Hardwired to 5333H	
02			**Device ID**	**24-2**
	15-0	R	Hardwired to 8C01	
04			**Command**	**24-2**
	0	R/W	Response to I/O space accesses enabled	
	1	R/W	Response to memory space accesses enabled	
	2	R/W	Enable bus master operation	
	3	R/W	Reserved	
	4	R/W	Capabilities list implemented	
	5	R/W	Enable DAC snooping	
	15-6	R/W	Reserved	
06			**Status**	**24-3**
	8-0	R/W	Reserved	
	10-9	R/W	Hardwired to select medium device select timing	
	11	R/W	Reserved	
	12	R/W	Received target abort	
	13	R/W	Received master abort	
	15-14	R/W	Reserved	
08			**Class Code**	**24-3**
	31-0	R	Hardwired to indicate VGA-compatible display controller and revision level	
0D			**Latency Timer**	**24-4**
	2-0	R/W	Reserved	
	7-3	R/W	Bus master latency timer	
10			**Base Address 0**	**24-4**
	0	R/W	Hardwired to indicate base registers map into memory space	
	2-1	R/W	Hardwired to allow mapping anywhere in 32-bit address space	
	3	R/W	Hardwired to indicate does not meet prefetchable requirements	
	22-4	R/W	Reserved	
	31-23	R/W	Base address 0	
2C			**PCI Configuration Space Subsystem ID**	**24-5**
	15-0	R	Subsystem vendor ID	
	31-16	R	Subsystem ID	

Table B-11. PCI Configuration Space Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
30			**BIOS Base Address**	**24-5**
	0	R/W	Enable access to BIOS ROM address space	
	15-1	R/W	Reserved	
	31-16	R/W	Upper 16 bits of BIOS ROM address	
34			**Capability Pointer**	**24-6**
	7-0	R/W	Hardwired to DCH	
3C			**Interrupt LIne**	**24-6**
	7-0	R/W	Interrupt line routing information	
3D			**Interrupt Pin**	**24-6**
	7-0	R	Use INTA or no interrupt	
3E			**Latency/Grant**	**24-7**
	7-0	R/W	Minimum grant	
	15-8	R/W	Maximum latency	
DC			**PCI Power Management Capability Identifier**	**24-7**
	7-0	R	Capabilites ID (hardwired to 01H)	
	15-8	R	Next Pointer (hardwired to 00H)	
DE			**PCI Power Management Capabilities**	**24-8**
	2-0	R	Version (hardwired to 01H)	
	4-3	R	Reserved	
	5	R	Device Specific Initialization (hardwired to 1)	
	8-6	R	Reserved	
	9	R	D1 state supported (hardwired to 1)	
	10	R	D2 state supported (hardwired to 1)	
	15-11	R	Reserved	
E0			**PCI Power Management Control/Status**	**24-9**
	1-0	R/W	Power state select	
	15-8	R	Reserved	

B.10 TV REGISTERS

Table B-12. TV Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
70			**TV Flicker Filter Control 1 (SR70)**	**25-1**
	0	R/W	Enable flicker filter	
	1	R/W	3 or 2 line flicker filter	
	2	R/W	Color space conversion format	
	3	R/W	Chroma filter disable	
	4	R/W	Active area select	
	5	R/W	Enable flicker filter for the secondary stream	
	6	R/W	Reserved	
	7	R/W	Output flicker filter on CRT DAC	
71			**TV Flicker Filter Control 2 (SR71)**	**25-2**
	2-0	R/W	Filtering fraction	
	3	R/W	Reserved	
	4	R/W	Luminance clipping	
	5	R/W	Luminance offset	
	6	R/W	Chromanance clipping	
	7	R/W	Enable 8-bit 4:2:2 YCbCr output to external encoder	
72			**TV Flicker Filter Control 3 (SR72)**	**25-3**
	0	R/W	Y filter only	
	1	R/W	Enable SIT	
	3-2	R/W	Aperture correction control	
	5-4	R/W	CRT/TV test mode (test only)	
	6	R/W	Flicker filter test mode 1 (test only)	
	7	R/W	Flicker filter test mode 2 (test only)	
73			**Set Interpretive Threshold (SR73)**	**25-4**
	7-0	R/W	SIT value	
74			**Aperture Correction (SR74)**	**25-5**
	7-0	R/W	Aperture correction value	
75			**Aperture Correction Low Threshold (SR75)**	**25-5**
	7-0	R/W	Aperture correction low threshold value	
76			**Aperture Correction Mid Threshold (SR76)**	**25-5**
	7-0	R/W	Aperture correction mid threshold value	
77			**Aperture Correction High Threshold (SR77)**	**25-6**
	7-0	R/W	Aperture correction high threshold value	

Table B-11. TV Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
78			**TV VSYNC Delay (SR78)**	**25-6**
	7-0	R/W	TV VSYNC delay bits 11-4	
79			**U-Burst (SR79)**	**25-6**
	7-0	R/W	U-Burst value	
7A			**V-Burst (SR7A)**	**25-7**
	7-0	R/W	V-Burst value	
7B			**Subcarrier to Pixel Clock Ratio 1 (SR7B)**	**25-7**
	7-0	R/W	Subcarrier to pixel clock ratio bits 7-0	
7C			**Subcarrier to Pixel Clock Ratio 2 (SR7C)**	**25-8**
	7-0	R/W	Subcarrier to pixel clock ratio bits 15-8	
7D			**Underscanning Control 1 (SR7D)**	**25-8**
	0	R/W	Underscanning method	
	1	R/W	Force 9-dot text to 8-dot	
	2	R/W	Enable underscanning on hardware cursor	
	3	R/W	Enable underscanning on hardware icon	
	7-4	R/W	Subcarrier to pixel clock ratio bits 19-16	
7E			**Underscanning Control 2 (SR7E)**	**25-9**
	7-0	R/W	Underscanning enable and start position	
	1	R/W	Underscanning interval	
7F			**Underscanning Control 3 (SR7F)**	**25-10**
	7-0	R/W	Underscanning offset	
80			**Color Space Conversion Factor 0 (SR80)**	**25-10**
	7-0	R/W	Color space conversion factor 0	
81			**Color Space Conversion Factor 1 (SR81)**	**25-10**
	7-0	R/W	Color space conversion factor 1	
82			**Color Space Conversion Factor 2 (SR82**	**25-11**
	5-0	R/W	Color space conversion factor 2	
	6	R/W	Reserved	
	7	R/W	Bit 8 of factor 1	
83			**Color Space Conversion Factor 3 (SR83)**	**25-11**
	7-0	R/W	Color space conversion factor 3	
84			**Color Space Conversion Factor 4 (SR84)**	**25-12**
	7-0	R/W	Color space conversion factor 4	
85			**Color Space Conversion Factor 5 (SR85)**	**25-12**
	5-0	R/W	Color space conversion factor 5	
	6	R/W	Reserved	
	7	R/W	Test Bit	

Table B-11. TV Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
86			**Color Space Conversion Factor 6 (SR86)**	**25-13**
	6-0	R/W	Color space conversion factor 6	
	7	R/W	Enable flicker filter on VSYNC	
87			**Color Space Conversion Factor 7 (SR87)**	**25-13**
	7-0	R/W	Color space conversion factor 7	
88			**Color Space Conversion Factor 8 (SR88)**	**25-14**
	7-0	R/W	Color space conversion factor 8	
89			**Software Scratch 0 (SR89)**	**25-14**
	7-0	R/W	Software scratch 0	
8A			**Software Scratch 1 (SR8A)**	**25-14**
	7-0	R/W	Software scratch 1	
8B			**Software Scratch 2 (SR8B)**	**25-15**
	7-0	R/W	Software scratch 2	
8C			**Software Scratch 3 (SR8C)**	**25-15**
	7-0	R/W	Software scratch 3	
8D			**Software Scratch 4(SR8D)**	**25-15**
	7-0	R/W	Software scratch 4	
8E			**Software Scratch 5 (SR8E)**	**25-15**
	7-0	R/W	Software scratch 5	
8F			**Software Scratch 6 (SR8F)**	**25-16**
	7-0	R/W	Software scratch 6	
90			**TV Parameter 0 (SR90)**	**25-16**
	7-0	R/W	TV Parameter 0	
91			**TV Parameter 1 (SR91)**	**25-16**
	7-0	R/W	TV Parameter 1	
92			**TV Parameter 2 (SR92)**	**25-17**
	7-0	R/W	TV Parameter 2	
93			**TV Parameter 3 (SR93)**	**25-17**
	7-0	R/W	TV Parameter 3	
94			**TV Parameter 4 (SR94)**	**25-17**
	7-0	R/W	TV Parameter 4	
95			**TV Parameter 5 (SR95)**	**25-18**
	7-0	R/W	TV Parameter 5	
96			**TV Parameter 6 (SR96)**	**25-18**
	7-0	R/W	TV Parameter 6	
97			**TV Parameter 7 (SR97)**	**25-18**
	7-0	R/W	TV Parameter 7	
98			**TV Parameter 8 (SR98)**	**25-19**
	7-0	R/W	TV Parameter 8	

Table B-11. TV Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
99			**TV Parameter 9 (SR99)**	**25-19**
	7-0	R/W	TV Parameter 9	
9A			**TV Parameter 10 (SR9A)**	**25-19**
	7-0	R/W	TV Parameter 10	
9B			**TV Overflow Parameter 0 (SR9B)**	**25-20**
	2-0	R/W	TV Parameter 0 bits 10-8	
	3	R/W	Reserved	
	6-4	R/W	TV Parameter 1 bits 10-8	
	7	R/W	Reserved	
9C			**TV Overflow Parameter 1 (SR9C)**	**25-20**
	2-0	R/W	TV Parameter 2 bits 10-8	
	3	R/W	Reserved	
	6-4	R/W	TV Parameter 3 bits 10-8	
	7	R/W	Reserved	
9D			**TV Overflow Parameter 2 (SR9D)**	**25-21**
	2-0	R/W	TV Parameter 4 bits 10-8	
	3	R/W	Reserved	
	6-4	R/W	TV Parameter 5 bits 10-8	
	7	R/W	Reserved	
9E			**TV Overflow Parameter 3 (SR9E)**	**25-21**
	1-0	R/W	TV Parameter 6 bits 9-8	
	3-2	R/W	TV Parameter 7 bits 9-8	
	5-4	R/W	TV Parameter 8 bits 9-8	
	7-6	R/W	Reserved	
9F			**TV Overflow Parameter 4 (SR9F)**	**25-22**
	2-0	R/W	TV Parameter 9 bits 10-8	
	3	R/W	TV encoder test mode 1 (test only)	
	6-4	R/W	TV Parameter 10 bits 10-8	
	7	R/W	TV encoder test mode 2 (test only)	

B.11 FLAT PANEL REGISTERS

Table B-13. Flat Panel Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**30**		**Architectural Configuration (SR30)**	**26-1**
	0	R/W	Select single or dual-scan panel	
	1	R/W	Streams Processor controller source	
	2	R/W	TV DAC controller source	
	3	R/W	DCLK select for Controller 1	
	4	R/W	DCLK select for Controller 2	
	5	R/W	Reserved	
	6	R/W	Flat panel text mode	
	7	R/W	Enable external TV encoder support on FPD[35:24]	
3C5	**31**		**Flat Panel Display Mode (SR31)**	**26-2**
	0	R/W	CRT test mode	
	1	R/W	Select flat panel data source	
	2	R/W	Select CRT DAC data source	
	3	R/W	CLUT test mode (test only)	
	4	R/W	Enable flat panel display	
	5	R/W	Reserved	
	6	R/W	Select hardware icon controller	
	7	R/W	Select hardware cursor controller	
3C5	**32**		**Flat Panel Polarity Control (SR32)**	**26-4**
	0	R/W	Reserved	
	1	R/W	CRT HSYNC polarity during simultaneous display	
	2	R/W	CRT VSYNC polarity during simultaneous display	
	3	R/W	FPDCLK polarity	
	4	R/W	Flat panel data polarity	
	5	R/W	FPDE polarity	
	6	R/W	FPHSYNC/LP polarity	
	7	R/W	FPVSYNC/FLM polarity	
3C5	**33**		**Flat Panel Function Control 1 (SR33)**	**26-5**
	0	R/W	Enable FPDCLK output	
	3-1	R/W	FPDCLk delay	
	4	R/W	Force 8-frame FRC	
	5	R/W	Enable hardware cursor/icon during screen off	
	6	R/W	Enable extra LP	
	7	R/W	Reserved	
3C5	**34**		**Flat Panel AC Modulation (SR34)**	**26-6**
	6-0	R/W	Clock period units for MOD pulse	
	7	R/W	Enable MOD output on pin B15	

Table B-13. Flat Panel Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**35**		**Flat Panel Function Control 2 (SR35)**	**26-6**
	2-0	R/W	FPGPIO function select	
	3	R/W	FPGPIO data	
	4	R/W	Mod clock select	
	5	R/W	Flat panel test mode 1 (test only)	
	6	R/W	Flat panel test mode 2 (test only)	
	7	R/W	General test mode 2 (test only)	
3C5	**36**		**Flat Panel Dither Control (SR36)**	**26-7**
	0	R/W	Select number of bits for dithering	
	2-1	R/W	Reserved	
	5-3	R/W	Select number of bits in the base color	
	7-6	R/W	Dither control	
3C5	**37**		**Flat Panel FRC Weight Select RAM (SR37)**	**26-8**
	3-0	R/W	Weight select value pointer	
	7-4	R/W	Reserved	
3C5	**38**		**Flat Panel FRC Weight Select RAM Data (SR38)**	**26-8**
	7-0	R/W	Weight select data	
3C5	**39**		**Flat Panel Algorithm Control (SR39)**	**26-8**
	1-0	R/W	Select STN or TFT panel type	
	2	R/W	Reserved	
	4-3	R/W	Select FRC gray levels	
	7-5	R/W	Reserved	
3C5	**3A**		**Flat Panel FRC Tuning 1 (SR3A)**	**26-9**
	7-0	R/W	FRC tuning data 15-8	
3C5	**3B**		**Flat Panel FRC Tuning 2 (SR3B)**	**26-9**
	7-0	R/W	FRC tuning data 7-0	
3C5	**3C**		**Flat Panel Test (SR3C)**	**26-9**
	1-0	R/W	Reserved	
	2	R/W	STN test mode (test only)	
	7-3	R/W	Reserved	
3C5	**3D**		**Flat Panel Configuration 1 (SR3D)**	**26-10**
	2-0	R/W	Data output format	
	3	R/W	Always leave progrmmed to 0	
	4	R/W	Disable LP and FPSCLK during vertical blank	
	5	R/W	Disable FPSCLK during first line of vertical blank	
	6	R/W	Select flat panel data drive strength	
	7	R/W	Select the FPSCLK drive stregth	

Table B-13. Flat Panel Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**3E**		**Flat Panel PWM1 Duty Cycle (SR3E)**	**26-11**
	7-0	R/W	PWM1 duty cycle	
3C5	**3F**		**Flat Panel FRC Tuning 3 (SR3F)**	**26-11**
	7-0	R/W	FRC tuning data	
3C5	**40**		**Flat Panel Dither Control (SR40)**	**26-11**
	0	R/W	Reserved	
	3-1	R/W	FPSCLK delay	
	4	R/W	Force flat panel data and control signals low	
	5	R/W	FPSCLK forced low during non-display interval	
	6	R/W	Double edge pixel clocking for TFT panels	
	7	R/W	Enable FPPOL output	
3C5	**41**		**Flat Panel Power Sequence Control (SR41)**	**26-12**
	0	R/W	Specifiy sync outputs	
	1	R/W	Reserved	
	2	R/W	Power down phase timing	
	3	R/W	Power up phase timing	
	5-4		Reserved	
	7-6	R/W	Standy timer resolution	
3C5	**42**		**Flat Panel Power Management Control (SR42)**	**26-13**
	0	R/W	Reserved	
	1	R/W	Enable software suspend	
	3-2	R/W	Reserved	
	4	R/W	Enable hardware standby	
	5	R/W	Enable software standby	
	7-6	R/W	Suspend debounce timer value	
3C5	**43**		**Flat Panel Standby Control (SR43)**	**26-14**
	5-0	R/W	Standby timer timeout value	
	6	R/W	Enable activity mode	
	7	R/W	Reserved	
3C5	**44**		**Flat Panel Power Management (SR44)**	**26-14**
	3-0	R/W	Reserved = 0000b	
	4	R	Specify STANDBY pin function	
	7-5	R	Reserved	

Table B-13. Plat Panel Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**45**		**Flat Panel PLL Power Management (SR45)**	**26-15**
	1-0	R/W	Suspend to PLL power down time	
	7-2	R/W	Reserved	
3C5	**46**		**Flat Panel Power Management Status (SR46)**	**26-15**
	4-0	R	Reserved	
	5	R	1 = in Standby mode	
	6	R	1 = in idle power down state	
	7	R	1 = in idle power up state	
3C5	**47**		**CLUT Control (SR47)**	**26-16**
	1-0	R/W	Select CLUT for reads and writes	
	7-2	R/W	Reserved	
3C5	**48**		**Icon Mode (SR48)**	**26-16**
	0	R/W	Enable hardware icon	
	1	R/W	Select icon mode	
	2	R/W	Double X size	
	3	R/W	Double Y size	
	7-4	R/W	Icon address bits 11-8	
3C5	**49**		**Icon Color Stack (SR49)**	**26-18**
	7-0	R/W	Values for four 24 bits/pixel colors	
3C5	**4A**		**Icon X Position High (SR4A)**	**26-19**
	1-0	R/W	High order 3 bits of icon horizontal position	
	7-2	R/W	Reserved	
3C5	**4B**		**Icon X Position Low (SR4B)**	**26-19**
	7-0	R/W	Low order 8 bits of icon horizontal position	
3C5	**4C**		**Icon Y Position High (SR4C)**	**26-20**
	1-0	R/W	High order 3 bits of icon vertical position	
	7-2	R/W	Reserved	
3C5	**4D**		**Icon Y Position Low (SR4D)**	**26-20**
	7-0	R/W	Low order 8 bits of icon vertical position	
3C5	**4E**		**Icon Address High (SR4E)**	**26-21**
	7-0	R/W	Icon address bits 19-12	
3C5	**4F**		**Dual-Scan STN Data Address (SR4F)**	**26-21**
	7-0	R/W	STN panel data start address adjustment	

Table B-13. Flat Panel Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**50**		**Dual-Scan STN Frame Buffer Size Low (SR50)**	**26-22**
	7-0	R	STN frame buffer size low byte	
3C5	**51**		**Dual-Scan STN Frame Buffer Size High (SR51)**	**26-22**
	7-0	R	STN frame buffer size high byte	
3C5	**52**		**Flat Panel PWM Register (SR52)**	**26-23**
	0	R/W	Enable PWM0	
	1	R/W	PWM source clock select	
	3-2	R/W	Reserved	
	6-4	R/W	PWM clock divide	
	7	R/W	ODD/PWM1 function enable	
3C5	**53**		**Flat Panel PWM0 Duty Cycle (SR53)**	**26-24**
	7-0	R/W	Specify PWM0 duty cycle	
3C5	**54**		**Flat Panel Horizontal Compensation 1 (SR54)**	**26-24**
	1-0	R/W	Text mode horizontal expansion	
	3-2	R/W	Graphics mode horizontal expansion	
	4	R/W	Enable horizontal centering	
	6-5	R/W	Reserved	
	7	R/W	Enable line graphics character codes	
3C5	**55**		**Flat Panel Horizontal Compensation 2 (SR55)**	**26-25**
	0	R/W	Enable 40-character text mode horizontal expansion	
	1	R/W	Enable 80-character text mode horizontal expansion	
	2	R/W	Enable 640-column graphics mode horizontal expansion	
	3	R/W	Enable 800-column graphics mode horizontal expansion	
	4	R/W	Enable 1024-column graphics mode horizontal expansion	
	6-5	R/W	Enable horizontal expansion filter	
	7	R/W	Alternate text mode horizonatal expansion	
3C5	**56**		**Flat Panel Vertical Compensation 1 (SR56)**	**26-26**
	1-0	R/W	Text mode vertical expansion	
	3-2	R/W	Graphics mode vertical expansion	
	4	R/W	Enable vertical centering	
	7-5	R/W	Reserved	

Table B-13. Flat Panel Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**57**		**Flat Panel Vertical Compensation 2 (SR57)**	**26-27**
	0	R/W	Enable 350-line text mode vertical expansion	
	1	R/W	Enable 200/400-line text mode vertical expansion	
	2	R/W	Enable 350-line graphics mode vertical expansion	
	3	R/W	Enable 200/400-line graphics mode vertical expansion	
	4	R/W	Enable 480-line graphics mode vertical expansion	
	5	R/W	Enable 600-line graphics mode vertical expansion	
	6	R/W	Enable 768-line graphics mode vertical expansion	
	7	R/W	Reserved	
3C5	**58**		**Flat Panel Horizontal Border (SR58)**	**26-28**
	7-0	R	Character clocks per horizontal line not used by video image	
3C5	**59**		**Flat Panel Horizontal Expansion Factor (SR59)**	**26-29**
	0	R	Bit 8 of SR58	
	3-1	R	Reserved	
	6-4	R	Horizontal expansion factor	
	7	R	Reserved	
3C5	**5A**		**Flat Panel Vertical Border (SR5A)**	**26-29**
	7-0	R	Number of lines not used by video image	
3C5	**5B**		**Flat Panel Horizontal Expansion Factor (SR5B)**	**26-30**
	0	R	Bit 8 of SR5A	
	1	R	Automatic vertical expansion detect	
	2	R	Automatic vertical centering detect	
	3	R	0 = Current scan line will be repeated on next scan line	
	6-4	R	Vertical expansion factor	
	7	R	Reserved	
3C5	**5C**		**Flat Panel Display Enable Position Control (SR5C)**	**26-31**
	3-0	R/W	Display enable start postion for Controller 1	
	7-4	R/W	Display enable start position for Controller 2 - Paired	
3C5	**5D**		**Flat Panel/CRT Sync Position Control (SR5D)**	**26-32**
	3-0	R/W	Sync start position for Controller 1	
	7-4	R/W	Sync start position for Controller 2 - Paired	
3C5	**5E**		**Flat Panel BIOS Scratch 1 (SR5E)**	**26-32**
	7-0	R/W	Reserved for BIOS	
3C5	**5F**		**Flat Panel BIOS Scratch 2 (SR5F)**	**26-33**
	7-0	R/W	character clocks/line - 5	

Table B-13. Flat Panel Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**60**		**Flat Panel Horizontal Total (SR60)**	**26-33**
	7-0	R/W	character clocks/line - 5	
3C5	**61**		**Flat Panel Horizontal Panel Size (SR61)**	**26-33**
	7-0	R/W	Horizontal panel resolution - 1	
3C5	**62**		**Flat Panel Horizontal Blank Start (SR63)**	**26-34**
	7-0	R/W	Character clock counter value at blank start	
3C5	**63**		**Flat Panel Horizontal Blank End (SR63)**	**26-34**
	4-0	R/W	Character clock counter value at blank end	
	7-5	R/W	Reserved	
3C5	**64**		**Flat Panel Horizontal Sync Start (SR64)**	**26-35**
	7-0	R/W	Character clock counter value at sync start	
3C5	**65**		**Flat Panel Horizontal Sync End (SR65)**	**26-35**
	4-0	R/W	Character clock counter value at sync end	
	6-5	R/W	Reserved	
	7	R/W	Horizontal sync end bit 5	
3C5	**66**		**Flat Panel Horizontal Overflow (SR66)**	**26-36**
	0	R/W	Flat panel horizontal total bit 8	
	1	R/W	Flat panel horizontal panel size bit 8	
	2	R/W	Flat panel horizontal blank start bit 8	
	3	R/W	Flat panel horizontal blank period greater than 64 char clocks	
	4	R/W	Flat panel horizontal sync start bit 8	
	5	R/W	Flat panel horizontal sync period greater than 32 char clocks	
	7-6	R/W	Reserved	
3C5	**68**		**Flat Panel Vertical Total (SR68)**	**26-37**
	7-0	R/W	Scan lines between vertical syncs - 2	
3C5	**69**		**Flat Panel Vertical Panel Size (SR69)**	**26-37**
	7-0	R/W	Vertical panel resolution - 1	
3C5	**6A**		**Flat Panel Vertical Blank Start (SR6A)**	**26-38**
	7-0	R/W	Scan line counter value at blank start - 1	
3C5	**6B**		**Flat Panel Vertical Blank End (SR6B)**	**26-38**
	4-0	R/W	Scan line counter value at blank end	
	7-5	R/W	Reserved	
3C5	**6C**		**Flat Panel Vertical Sync Start (SR6C)**	**26-39**
	7-0	R/W	Scan line counter value at sync start - 1	
3C5	**6D**		**Flat Panel Vertical Sync End (SR6D)**	**26-39**
	3-0	R/W	Scan line counter value at sync end	
	7-4	R/W	Reserved	

Table B-13. Flat Panel Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**6E**		**Flat Panel Vertical Overflow 1 (SR6E)**	**26-40**
	2-0	R/W	Flat panel vertical total bits 10-8	
	3	R/W	Reserved	
	6-4	R/W	Flat panel vertical panel size bits 10-8	
	7	R/W	Reserved	
3C5	**6F**		**Flat Panel Vertical Overflow 2 (SR6F)**	**26-40**
	2-0	R/W	Flat panel vertical blank start bits 10-8	
	3	R/W	Reserved	
	6-4	R/W	Flat panel vertical sync start bits 10-8	
	7	R/W	Reserved	

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